37th International Conference on VLSI Design & 23rd International Conference on Embedded Systems

VLSI meets AI & Quantum for Cyber Physical Systems

6-10 January, 2024 | ITC Royal Bengal, Kolkata, India

VLSI Society of India

CALL FOR PAPERS

The world of Cyber Physical Systems (CPS) is transforming our industry and lives by connecting the physical world with the cyber components in an unprecedented manner. Rapid proliferation of CPS has led to the emergence of Industry 4.0 - the fourth industrial revolution that promises a new era in intelligent autonomy. The convergence of these systems with artificial intelligence technologies is fuelling powerful edge and cloud computing solutions. Similarly, quantum science and technologies are bringing new communication, sensing and secure data processing capabilities to CPS. It may be emphasized that our semiconductor industry remains a pivot to enable these key technologies, offering both opportunities and challenges, that when overcome can solve global problems in the field of agriculture, energy, climate, transportation, education, and healthcare. The conference aims at unearthing these issues for researchers and practitioners to see how VLSI and embedded systems can play a key role in enabling these ushering technologies.

VLSID 2024 provides a platform for industry and academia alike to discuss, deliberate and delve into the frontiers in semiconductors that could eventually enable disruptive technologies for the next generation. Original, unpublished papers describing research in the general areas of VLSI and hardware design are solicited in the following areas (but not limited to):

Topics:

- Hardware for Machine Learning and Artificial Intelligence
- Analog & Mixed Signal and, RF Circuits
- Embedded Systems, Internet of Things (IoT), and Cyber-Physical System (CPS) Design
- Hardware and Systems Security
- Test, Verification, and Reliability
- Electronic Design Automation
- Advanced process and Material, Device design and modelling
- Sensors, Packaging, and Interconnects
- Photonic Integrated Circuits, Wireless systems 5G and beyond, and Optical Communication
- Emerging Computing & Post-CMOS Technologies
- Low power Digital Systems
- Power and Energy Management
- VLSI for Automotive Systems
- Emerging Memory Technologies
- Quantum computing

Full Paper Submission Deadline : ~~30th July 2023~~ **21st August, 2023**
Notification for Acceptance : **On or Before 05th October, 2023**
Camera-ready manuscript: : **20th October 2023**

For Enquiry: **www.vlsid.org**
Submission Link: https://softconf.com/n/vlsid2024

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Previously published papers or papers currently under review for other conferences/journals should NOT be submitted and will not be considered. Electronic submission in PDF format to the **http://www.vlsid.org** website is required. Author and contact information (name, affiliation, mailing address, telephone, fax, e-mail) must be entered during the submission process. Paper Format: Submissions should be in camera-ready two-column format, following the IEEE proceedings specifications.

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentations at the conference. Every accepted paper MUST have at least one author registered to the conference by the time the camera-ready paper is submitted; at least one of the authors is also expected to attend the symposium and present the paper.

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Artificial Intelligence (AI) / Machine Learning (ML) Hardware: All aspects of AI algorithms and their hardware implementation;System, architecture, and circuit-level innovations for AI/ML; AI accelerator design; AI boosted circuits and systems for Brain Machine Interface (BMI); Intelligent storage; Memory-centric accelerator design;Autonomous systems; Trusted architectures for AI;Neuromorphic computing;Brain-inspired computing and communication.

Analog, Mixed-Signal, and RF Circuits: Amplifiers, comparators, oscillators, filters, references; Nonlinear analog circuits; Digitally-assisted analog circuits; Analog design at lower technology nodes; Analog circuits for diverse applications; Data Converters; PLL/ADPLL; I/O Design;Bio-inspired analog and mixed signal circuits; Analog circuits and instrumentation related to Biomedical, healthcare, sensor interfacing, wearable and flexible systems; Low Noise Circuits; EMI Immune Design; Auto Calibration Techniques; Wearable electronics;Flexible electronics;Ultra-low power circuit techniques; High Speed Interfaces, RF, mm-Wave and THz transceivers, SoCs, and SiPs; Frequency synthesizers;System architecture for 5G and 6G wireless, next generation systems for radar, sensing, and imaging; Reliability aspects in RFICs and building blocks for transceivers.

Embedded Systems, Internet of Things (IoT), and Cyber-Physical System (CPS) Design: Embedded Systems Language (ESL); System-level design methodology; Concurrent interconnect; Networks-on-chip; Defect-tolerant architectures; Hardware/Software co-design and co-verification; Reconfigurable computing; Embedded multicores and multiprocessor system on a chip(MPSoC); Real-time embedded systems; Embedded software including Operating Systems, Firmware, Middleware; Communication, virtualization, encryption, compression, security, reliability; Embedded systems for automotive and Electric Vehicles (EVs); Edge intelligence;Artificial Intelligence of Things (AIoT); Design automation for IoT/CPS; MedTech devices and systems.

Hardware and Systems Security: Secure and trustworthy hardware;Microelectronics supply chain security; Side-channel Attack (SCA); Fault injection attacks and mitigation; Hardware IP protection; Hardware Trojan attacks and mitigation; Security of IoT/CPS; Firmware and software security; Secure cryptography; Automotive security; Security of multi-tenant systems; Scan protection; Row hammer attacks and mitigation; Physically Unclonable Functions (PUFs); Hardware design for Fully Homomorphic Encryptions (FHE); Micro-architectural security; Security of emerging devices and systems.

Test, Verification, and Reliability: Simulation, formal verification, validation at different abstraction levels; Hardware emulation;Design for Test (DFT); fault modelling and simulation; ATPG and BIST;Post-silicon validation and debug;Delay test and speed-binning;Memory test, Reliability and fault tolerance; 2.5D/3D IC testing; Analog and Mixed-signal testing; Static/dynamic defect- and fault-recoverability; Learning-assisted testing; Statistical Testing; Variation-aware design.

Electronic Design Automation (EDA): Logic and behavioral synthesis;Logic mapping, simulation and formal verification;Physical design techniques;Post-route optimizations; memory compiler;Simulation tools for design verification; Static Timing Analysis and timing exceptions; Mixed-Signal simulations; EDA for sub-10nm nodes; Design for Debug (DFD)tools; Application of AI/ML in CAD for VLSI; CAD for printed circuit boards (PCBs), CAD for secure chips.

Advanced Process/Material, Device Design and Modelling: Advanced CMOS process;Low-dimensional materials and devices; Meta-Materials; 2D and nanowire devices; Nano-patterning; Directed self-Assembly; EUV, ALE and selective deposition;Strain/channel engineering; Advanced manufacturing technology; Fabrication of Nano-Sensors and Bio-Sensors; metrology and yield; Deep nanoscaleCMOS devices; Device modeling and simulation; Multi-domain simulation; device/circuit-level reliability and variability; Devices for beyond CMOS, compact modeling and novel TCAD solutions, GaN and SiC devices for High Voltage applications, Design for Manufacturing (DFM) and Design for Yield (DFY).

Sensors, Packaging, and Interconnects: Methodologies and tools for Wafer-level packaging; Embedded chip packaging; 2.5D/3D integration with Silicon, SiCand Glass interposer; Thermal characterization and simulation; Component, system and product-level thermal management and characterization; Au/Ag/Cu/Al Wire-bond/Wedge bond technology; Flip-chip and Cu pillar; Solder alternatives; Cu to Cu, wafer-level bonding and die attachment (Pb-free), Fan-out, panel-level, chiplets, SiP, micro-bump, high I/O thermo compression /hybrid bonding; fine-pitch/multi-layer RDL; Printable interconnects.

Photonic Integrated Circuits, Wireless systems 5G and beyond, and Optical Communication: Silicon and III-V Photonic Integrated Circuits; Wave guides /interconnects; On-chip lasers; Optical Multiplexers/Demultiplexers; Photodetectors and sensors; Quantum photonics, RF Photonics, Mid-IR/THz Photonics; Heterogeneous integration; Packaging of photonic devices; Quantum photonics; RF Photonics Mid-IR and THz Photonics; Receivers/ transmitters/ transceivers for wireline systems; Exploratory I/O circuits for advancing data rates, bandwidth density, power efficiency, equalization, robustness, adaptation capability,and design methodology.

Emerging Computing and post-CMOS Technologies: Quantum InformationProcessing Systems; Quantum logic circuits; Quantum algorithms; Spin-based computing; Reversible computing; Approximate and stochastic computing; Cryogenic processors; MEDA; Microfluidic Biochips; Emerging memory technologies (ReRAM, Memristor, MRAM, FeRAM. nanotube RAM, phase-change memory); MEMS/NEMS devices andapplications; Electronics for automotive systems; Device, circuit, architecture design, analysis and optimization for neuromorphic computing systems.

Low-power Digital Systems: Next generation digital circuits, building blocks, and complete systems (monolithic, 2.5D, and 3D) for reduced power and form factor; Near- and sub-threshold systems; Energy-efficient algorithms and applications; Energy-efficient storage systems; Digital circuits for intra-chip communication; Clock distribution; Low-power and robust design; Digital regulators and digital sensors; Low-power autonomous systems; Low-power communication; Advances in memory architectures for power reduction; Design for low-power FPGA, GPU, NPU and TPU.

Power and Energy Management: Power management and controlcircuits, Regulators; Power converter ICs; Energy harvesting circuits andsystems; Wide-bandgap topologies and gate-drivers; Power and signalisolators;Powermanagementforautomotivesystems; Battery managementcircuits and systems; Power Delivery Networks (PDN); Power Switches; High Voltage Circuits and Systems; Power management for High Voltage Application; Power/Thermal balance.