1 Abstract:

The energy efficiency of computer architecture has been a challenge that drives the research in this domain. This challenge can be addressed from multiple directions, such as design methods, tools and technologies. This tutorial covers these aspects from basic to advanced levels for the design and development of future-generation low-power computer architectures. The description of the three tutorial talks is as follows:

Talk 1 (Farhad Merchant): The classical von Neumann computing model has a major shortcoming in terms of energy efficiency as it requires moving data among the various levels of memories. A practical solution to minimize these data movements is to perform computations as close to the memory as possible or inside the memory elements. While near-memory computing exhibits certain advantages, it still needs to improve as data movements are truncated and not minimized. On the other hand, in-memory computing is a novel paradigm that allows performing computing inside the memory resulting in a significant reduction of these data movements. Various technologies such as resistive random-access memory (ReRAM), magnetic random-access memory, and phase-change memory (PCM) are explored for performing computation in memory. In this talk, I will cover various design methods and tools developed by my group for ReRAM-based in-memory computing. I will discuss digital, analog and multi-bit computing paradigms in the first part. It was recently demonstrated that the classical stateful logic implementations (e.g., MAGIC) yield, on average, 68x higher energy than literature-reported results. In the second part, I will discuss formal verification methodologies for in-memory computing, where the correctness of the mapping of logic operations is examined. Finally, I will discuss hardware prototyping efforts that complement the simulation and verification methodologies.

Talk 2 (Rolf Drechsler): Traditionally, the tool flow for the realization of digital circuits was purely design-centred, i.e. ensuring the quality through testing and verification was essentially considered as a post-processing step. To this end, mainly approaches based on simulation have been applied in the past. But the growing complexity according to Moore's law showed the need for more powerful solutions. In the mid-80s, formal techniques have been proposed as a proper alternative – first in the area of verification. In the meantime, elaborated methods exploiting formal methods increasingly find application in industrial practice. This success was possible due to the improvements of the underlying solve engines, but also due to a better understanding of how to effectively apply them. Motivated by these results, applications of formal techniques beyond verification have been studied.

The talk gives an overview of the development of solve engines over the past two decades. It is shown how the core techniques work and what the core paradigms behind a successful automatic engine are. Not only Boolean techniques, like BDD and SAT, are presented, but also extensions to word-level descriptions for decision diagrams and solve engines exploiting additional theories.

Talk 3 (Vikas Rana): In modern society, data has become an indispensable part of human life. The rate at which the data is generated is exploding. This is not only pushing our current computation technologies to their limits, but also that of our energy production: ICT and data centers already consume around 8% of the world electricity production with an annual increase of 10%. This will soon become unsustainable. Therefore, we need new ways of computing. Neuromorphic computation could be an alternate way of computation which not only enhances the computation capability but also reduces the power consumption. The neuromorphic computation eliminates the bottleneck of today's computer architecture, given by Von Neumann, where memory and computation are separately located. In new architecture, the computation itself is done with-in-memory element. Redox based resistive switching (RRAM) device is a promising candidate for neuromorphic applications. These devices can store data for 10 years and switch as fast as 100ps. Multi-level switching capability of the devices further improves the computation capabilities in ternary or quandary logic system. The objective of this tutorial is to present the current understanding of the physical mechanism of memristve RRAM and address technological opportunities and challenges of ReRAM devices.

2 Speaker Biographies:

Farhad Merchant received his Ph.D. from the Indian Institute of Science, Bangalore (India), in 2016. His Ph.D. thesis title was "Algorithm-Architecture Co-design for Dense Linear Algebra Computations." He received the DAAD fellowship during his Ph.D. He worked as a postdoctoral research fellow at Nanyang Technological University (NTU), Singapore, from March 2016 to December 2016. In December 2016, he moved to Corporate Research at Robert Bosch in

Bangalore as a Researcher, where he worked on numerical methods for ordinary differential equations. He joined Institute for Communication Technologies and Embedded Systems, RWTH Aachen University, in December 2017 as a postdoctoral research fellow in the Chair for Software for Systems on Silicon. Farhad is the recipient of the HiPEAC technology transfer award in 2019 and the best paper award at ISQED 2022. Currently, Farhad is a Lecturer (Assistant Professor) at Newcastle University in the UK.

Rolf Drechsler received the Diploma and Dr. phil. nat. degrees in computer science from the Johann Wolfgang Goethe University in Frankfurt am Main, Germany, in 1992 and 1995, respectively. He worked at the Institute of Computer Science, Albert-Ludwigs University, Freiburg im Breisgau, Germany, from 1995 to 2000, and at the Corporate Technology Department, Siemens AG, Munich, Germany, from 2000 to 2001.

Since October 2001, Rolf Drechsler has been a Full Professor and Head of the Group of Computer Architecture, Institute of Computer Science, at the University of Bremen, Germany. In 2011, he additionally became the Director of the Cyber-Physical Systems Group at the German Research Center for Artificial Intelligence (DFKI) in Bremen. His current research interests include the development and design of data structures and algorithms with a focus on circuit and system design. He is an ACM Distinguished Member and an IEEE Fellow.

From 2008 to 2013 he was the Vice Rector for Research and Young Academics at the University of Bremen. Since 2018 he is the Dean of the Faculty of Mathematics and Computer Science.

Rolf Drechsler was a member of Program Committees of numerous conferences including e.g., DAC, ICCAD, DATE, ASP-DAC, FDL, MEMOCODE, and FMCAD. He was Symposiums Chair at ISMVL 1999 and 2014, and the Topic Chair for "Formal Verification" at DATE 2004, DATE 2005, DAC 2010, and DAC 2011 and 2018. He was the General Chair of the IEEE European Test Symposium 2018 and the Program Chair of ICCAD 2020. He received best paper awards at the Haifa Verification Conference (HVC) in 2006, the Forum on specification & Design Languages (FDL) in 2007, 2010 and 2020, the IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) in 2010, the Euromirco Digital System Design Conference 2020 and the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) in 2013 and 2018. He received the Berninghausen Award for Excellence in Teaching in 2018.

He is a co-founder of the Graduate School of Embedded Systems and he is the coordinator of the Graduate School "System Design" funded within the German Excellence Initiative. He is a co-founder and the spokesperson of the Data Science Center at the University of Bremen.

Rolf Drechsler served as an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration Systems, Chip, IET Cyber-Physical Systems: Theory & Applications, International Journal on Multiple-Valued Logic and Soft Computing, and ACM Journal on Emerging Technologies in Computing Systems.

Dr. Vikas Rana received his PhD from Delft university of Technology, Netherlands and worked at Philips semiconductor, Nijmegen and Indian Institute of Technology, New Delhi. From 2011, he has been leading a technology development group at Forschungzentrum, Germany. His main research interests include emerging ReRAM memory devices and integration with the contemporary CMOS technology. His research has been published in well renowned journals, Nature Nanotechnology, Advanced function Materials, IEEE TED etc. In 2017, his research on “computation with memory” has been cited by the Economist magazine. Further, he contributed a chapter titled “Redox-Based Memristive Devices” in “Memristors and Memristive Systems” book published by Springer New York.