

Tutorial Title:

Semiconductor Lithography and Process Scaling Methods from 65 nm to 2 nm

Abstract:

The rapid and exponential growth in electronics systems has been driven - more than anything else, by the ability of semiconductor manufacturers to rapidly shrink the processes. This has allowed integrated circuits to pack in progressively larger functionality with higher performance at a lower per-transistor cost.

This tutorial will cover the resolution limit of traditional optical lithography and the use of various resolution enhancement techniques (RETs), which allow the creation of shapes much smaller than these limits. The tutorial will briefly cover the RETs used before 20nm and will cover RETs for 20nm and below in greater detail. It also talks about how these RETs are used to create wires, transistors, and vias.

Until 20nm, various considerations for these RETs were limited to the manufacturing sides. However, after 20nm, the use of radical RETs has significantly influenced and impacted the design methodologies. The talk will also cover these design challenges and how modern design methodologies are taking care of these challenges.

Tutorial also throws light upon the advantages and challenges of FinFETs and further evolution of modern FETs such as GAAs and beyond.

Toward the end, we will also talk about the future of Moore's law. We will discuss various possibilities like "Moore's law is dead" or "it will continue using design-level innovations in the absence of process shrinking."

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Lead Speaker's Biography:

Sachin Shrivastava
Software Engineering Director
Cadence Design Systems
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Sachin has 21 years of industry experience and is currently working as Software Engineering Director in Cadence Design Systems, managing various R&D teams within the Virtuoso organization.

He received his M. Tech. in Communications Technology from IIT Kanpur. Before joining Cadence, he was working with Texas Instruments.

He holds 11 US patents and has published 12 technical papers at various international conferences like VLSID, ISQED, and ASPDAC. His areas of interest are Lithography, Semiconductor manufacturing, Design rules checking, Statistical timing, and crosstalk analysis.

Sachin is a recipient of Cadence Achievement Award, which is the highest level of recognition in Cadence.

Other Speaker's Biography:

Vishal Rastogi
Senior Principal Software Engineer
Cadence Design Systems
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Vishal has 20+ years of industry experience, which includes 14+ years working on multiple Electronic Design Automation tools with Cadence Design Systems. He is currently focusing on new tech node challenges related to design rules and leading the efforts to enable the new tech nodes within the Virtuoso®.

Vishal completed his B.Tech. in Computer Science and Engineering from Motilal Nehru National Institute of Technology (MNNIT), Allahabad, and an MBA from IIM Lucknow.

He has filed a patent on advanced cut-metal insertion and has published a paper on layout methodologies to address the effect of process variations on FinFET. He has been actively participating as an organizer or judge in various events organized by Cadence, other corporates, and the Government of India.