- **Tutorial Title:** Digital Design Verification - Objectives, Practices and Advanced Trends
- **Abstract:**

As VLSI designs become increasingly complex, so does the challenge to **ensure that designs meet architectural specification requirements**. Design verification is an important aspect of product development and consumes as much as **80%** of total product development time. This includes activities done in different stages namely Pre-silicon verification, Pre-silicon validation (emulation), Post-silicon validation and Production testing. Each of these activities is done with a different set of objectives.

The tutorial will start with enlisting these objectives and then move on to explain various practices widely adopted in the industry to achieve these objectives. Focus will be predominantly on pre-silicon functional verification.

This tutorial will discuss the functional verification techniques classified based on:

- Design granularity - IP vs SoC vs Subsystem
- Methodology – Simulation vs Formal methods
- Stimulus - Directed vs Constrained Random
- Checker – Self-Checking vs Model Based vs Assertions

Other verification methods that augment the above will also be discussed:

- Gate Level Simulations, Analog Mixed Signal (AMS) verification, Clock/Reset Domain Crossing (CDC/RDC) verification, Code and Functional Coverage metrics, Production testing with Functional vectors, IO Timing Verification

The tutorial will move on to elucidate some of the emerging advanced trends in the industry.

Trend #1: Formal verification (FV) - Applications and advancements

a. *Different FV application areas*
   - X-Propagation, CDC-RDC verification, Sequential Equivalence Checks (SEC), Datapath verification, Register verification, Security verification, Coverage metrics

b. *Convergence problem and resolution techniques*
   - Simplifying assumptions, Submodule verification, Defining cut points, Proof-structuring, Bounded proof, Bug hunting, Proof caching and ML training of proof engines, Counter and FIFO abstractions

c. Choosing between Formal vs Dynamic verification techniques for a given design.

Trend #2a: Machine Learning (ML) based coverage closure acceleration

Simulation based verification of a complex design requires huge set of test cases, which need to be run multiple times, in order to achieve 100% coverage with randomization, thereby resulting in huge run times. Test run database size also increases proportionately with the number of runs. These issues can be mitigated by modern-day simulators built on ML techniques. The idea

is to achieve coverage with a smaller number of testcase runs while preserving randomization nature of testcases. This section discusses the process of achieving this reduction in testcases (stimuli).

Trend #2b: ML based Fault analysis acceleration

Increasing safety criticality of systems and applications has led to the need for protective measures ensuring functional safety (FuSa). The important aspect in designing systems for highest Safety Integrity Levels (SIL) is identification of vulnerable nodes that can lead to potential failures. Traditionally, system reliability in mission mode is evaluated using Fault injection (FI), which is a strategy used to determine the effectiveness of Safety Mechanisms (SMs) in a safety critical system. FI done on semiconductor components is a challenging process due to increasing complexity of designs, which leads to high resource demands and simulation time overheads. A combination of structural analysis and ML based framework can help in predicting critical nodes in hardware designs, and can bring down the overheads of FI. This section discusses this strategy in detail.

Karthik Rajakumar leads the IP DV team in the C2000 MCU Group at Texas Instruments India and is also a Member Group Technical Staff (MGTS) at TI. He has an experience of 17 years in the fields of IP and SoC Design Verification, RTL Design, and Architecture Specification. He specializes in the areas of CPU and HW Safety/Security verification. Prior to TI, he worked for Nokia-Renesas Mobile and Montalvo Systems. He holds a Bachelor's degree in Electronics and Communication Engineering from College of Engineering, Guindy, Anna University and a Master's degree in Embedded Systems from BITS, Pilani. He has delivered invited talks on Digital Design Verification at IIT-Hyderabad, IIT-Tirupati and National University of Singapore.

Naveen Kothuri is an RTL design engineer working with the C2000 MCU Group of Texas Instruments and has been with TI for more than 5 years. He has worked on designing multi-clock domain IPs and interconnects of C2000. His major interest areas include Formal verification, Signal processing, IP design, System Architecture and prototyping. He holds a Bachelor's degree in Electrical Engineering from SRKR Engineering College, Bhimavaram and a Master's degree in Electrical Engineering from Indian Institute of Technology, Madras.

Bhavya Dasari is a DV engineer working with the C2000 MCU Group of Texas Instruments, with more than 7 years of experience in the Design Verification domain. She has used both UVM and Formal tools to verify multiple IPs across her career and is an expert in CPU verification, coverage and data path verification. She graduated from NIT Trichy with a Bachelor's degree in Electronics and Communication.

Pooja Madhusoodhanan is a DV engineer working with the C2000 MCU Group of Texas Instruments, with more than 6 years of experience across SoC DV, IP DV, SV-UVM, Formal verification and IP architecture. She also has expertise in Functional Safety Verification. She graduated from NIT Trichy with a Bachelor's degree in Electrical and Electronics.

All the speakers have presented several papers/posters in the areas of Digital Design Verification, in TI internal conferences and external conferences like DAC, IEEE Wintechcon, VLSID, DVCon and CadenceLIVE.