Tutorial Title: **Designing Efficient and Secure NoC-based Heterogeneous SoCs**

Abstract:
To meet the needs of the real-time processing architectures, the embedded systems are moving toward heterogeneous System-on-Chip (SoC) design. Alongside the general-purpose cores, the heterogeneous SoCs include application-specific customized designs, commonly known as hardware accelerators, which accelerate the performance of specific functions and provide energy efficiency. All the processing elements share the on-chip resources like memory etc., and communicate with each other through a shared Network-on-chip (NoC). The growing system sizes and time-to market pressure of accelerator-rich heterogeneous SoCs compel the chip designers to analyze only part of the design space, leading to suboptimal Intellectual Property (IP) designs. Hence, the accelerators are generally designed as standalone IP blocks by third-party vendors and chip designers often over-provision the amount of on-chip resources required to add flexibility to each accelerator design. Although this modularity simplifies IP design, integrating these off-the-shelf accelerator blocks into a single SoC may overshoot the resource budget of the underlying system. However, integrating the third-party IP blocks into the system may lead to various security vulnerabilities, which are hard to detect. Firstly, the lack of design details from the third-party vendors makes it hard to validate the IP blocks. Secondly, even with the design details, it becomes infeasible to exhaustively explore the millions of logic elements to find a possible design bug or malicious modifications like Hardware Trojans (HTs). In this tutorial we will highlight and address the challenges involved in designing efficient accelerator-rich SoCs by optimizing the utilization of on-chip resources and mitigating the aforementioned performance-based security threats. We will describe a few security attacks in detail and discuss the state-of-the art attack detection and localization techniques. Moreover, with the integration of several processing elements, the contemporary systems are becoming extremely complex in their design. Validating such modules is really challenging at the post-silicon debug phase. In this tutorial, we will discuss how augmented wireless capability to the traditional NoC can provide efficient design-for-debug infrastructure to validate such designs. Additionally, we shall discuss the reusability of the debug infrastructure for different architectural purposes to minimize the overhead associated with the debug infrastructure while gaining performance improvement.

Speakers:

Dr. Sujay Deb:

Sujay is a Professor in Dept. of Electronics and Communication Engineering and Dept. of Computer Science and Engineering at Indraprastha Institute of Information Technology, Delhi (IIIT-D). He is also serving as the Dean of Student Affairs. He received PhD from the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA on May 2012. His research Interests are broadly in the areas of power and performance efficient and reliable System-on-Chip Design, Network-on-Chip (NoC) communication fabrics, Heterogeneous System Architectures (HSA), hardware for deep learning, low-cost bio-sensors for preventive healthcare.

Dr. Subhra Kanti Das:

Subhra is currently the Head of Research and Technology at Thales' Engineering Competence Center (ECC) based in Bangalore. In his current role, he is driving the eco-system in India for RISC-V research and technology enhancement as part of Thales global strategy towards open hardware. He is steering multiple collaborations with academic institutions along with nodal Govt R&D organizations in India and with OpenHW Consortium, Thales Research and Technology centers in France, Singapore and Canada. His current area of work and interests are Safety NoC for multi-core systems, Security implications for embedded systems and Generative AI. He received his PhD from Jadavpur University, Kolkata, India in 2016.

Dr. Mitali Sinha:

Mitali is currently working as a researcher in Shell India Markets Pvt. Ltd, Bangalore, India. She is a part of the Digital and Scientific High Performance Computing team, and is working on performance optimization of complex large-scale scientific applications. Before joining Shell, she worked as a researcher in Computer Systems Architecture, R&D unit at IMEC, Belgium. She received her PhD degree in Computer Science and Engineering from Indraprastha Institute of Information Technology Delhi (IIITD), India, in 2022. She holds gold medals in both Bachelor's and Master's degrees. She was awarded "Dean IRD Research Excellence Award, IIITD, 2022" and "Best Student Research Forum Award at VLSID 2022" for her PhD Thesis.

Dr. Sidhartha Sankar Rout:

Sidhartha is currently working as a Technical Leader in STMicroelectronics, Greater Noida, India. His current focus is on the development of power efficient AI hardware. He has completed his PhD degree from IIIT Delhi in the year 2023. During his PhD, his research focus was to develop efficient debug architectures for the validation of NoC sub-system. He has won the VLSID 2021 SRF Award and ASPDAC 2021 SRF Best Poster Award for his research contributions during his PhD.