

VLSI Sensors, Circuits, and Systems for Particle Physics Experiments

Abstract: VLSI sensors, circuits, and systems have played a pivotal role in modern particle physics experiments, including the discovery of the Higgs boson at CERN in 2012. The CMS and ATLAS detectors within the Large Hadron Collider (LHC) that finally sensed the elusive Higgs boson are essentially giant high-speed cameras (the largest ever built) constructed around the interaction points of beams of high-energy protons. Each detector is about 40 m long, has a diameter of 20 m, and contains many types of sensors organized into several concentric layers. The innermost layer, known as the silicon vertexing and tracking (SVT) layer, contains an array of Si-based monolithic active pixel sensors (MAPS) that covers a total area of $\sim 200 \text{ m}^2$ and includes millions of sensing channels (pixels) for reconstructing the paths of particles originating from the interaction points. A variety of custom CMOS ASICs are used to read out the pixels, provide on-line selection of potentially interesting events, and transfer data to an FPGA-based data acquisition system (DAQ). The design of these chips is challenging for many reasons, including 1) strict power consumption limitations; 2) high levels of ionizing radiation (orders of magnitude higher than for space applications); and 3) high data rates ($\sim 40 \text{ TB/s}$ before event selection). Future experiments, such as the high-luminosity LHC (HL-LHC) and the electron-ion collider (EIC), will result in even higher radiation levels and/or data rates, further increasing the associated design challenges. Other particle physics experiments (not based on accelerators) also require VLSI for sensing and computing but have different operating environments. Rare-event searches, which aim to detect elusive, low-probability events such as neutrino interactions and hypothesized neutrinoless double-beta decays, generally operate in ultra-low-radiation environments at cryogenic temperatures. For example, the four “far” neutrino detectors planned for the Deep Underground Neutrino Experiment (DUNE) will operate underground within 70,000 tons (70 kTon) of ultrapure liquid Argon at 84K. Each 10 kTon detector has 3,000 128-channel front-end (FE) motherboards containing a total of 54,000 FE ASICs that feed 12,000 1.28 GB/s data links (resulting in a raw data rate of 9.2 Tb/s).

The proposed tutorial aims to introduce participants to the wide variety of applications for high-performance VLSI design in modern physics experiments, including precision sensing, energy-efficient and fault-tolerant computing and communications, and real-time machine learning (ML). Specific topics that will be discussed include 1) an introduction to monolithic sensors for photons and charged particles; 2) integrated quantum sensors; 3) effects of radiation on analog and digital ICs; 4) cryogenic operation of analog and digital ICs; 5) design of low-noise and cryogenic analog front-ends (AFEs); 6) introduction to high-speed wired and optical data links; 7) techniques for fault-tolerant digital VLSI design; and 8) high-level synthesis of on-chip real-time digital signal processing (DSP) and ML algorithms. The use of modern CAD tools will be emphasized throughout using step-by-step examples. Various free tools will also be demonstrated live (if time permits), including TMRG (for incorporating redundancy into digital designs) and hsl4ml (for high-level synthesis of ML algorithms into FPFAs and ASICs).

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Speaker Bio: Soumyajit Mandal (Senior Member, IEEE) received the B.Tech. degree in electronics and electrical communications engineering from IIT Kharagpur, Kharagpur, India, in 2002, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2004 and 2009, respectively. He was a Research Scientist with Schlumberger-Doll Research, Cambridge, from 2010 to 2014, an Assistant Professor with the Department of Electrical Engineering and

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