Tutorial Proposal
VLSI Design 2024

Recent Advances in Test: Cell Aware and Timing Aware Fault Models, and Component System Level Tests

Abstract:

This tutorial presents recent advances in digital VLSI Test methodologies that are aimed at delivering very low DPPM levels in screened parts fabricated in state-of-the-art cutting-edge technologies. We begin with an in-depth look at structural scan based Stuck-at and TDF tests to understand the potential sources of test escapes from these traditional test methods. We then explain how new Cell Aware and Timing Aware fault models are being employed to generate additional scan tests to plug the test coverage holes during testing. Test prioritization approaches, based on layout design-for-manufacturability information and critical area analysis, will also be explained; these are being concurrently developed to systematically manage and reduce the significant growth in test patterns due to the new tests, and thereby limit the increase in test application time and costs. However, even these new fault models are often unable to ensure acceptable quality for the many complex SOCs tested solely using low-cost scan structural tests. We also describe the expensive functional level system level tests, applied on the fully packaged part, that are now widely used as a final test screen to further reduce test escapes to reach desired defect levels. Finally, some failures escape even the most stringent pre-deployment testing, and cause malfunction in operation; silent data errors in datacenters is an example that has received considerable publicity in recent months. In concluding the tutorial, we will discuss the characteristics of such test escapes that may go undetected during testing and cause failures in the field.

Presenter:

Adit D. Singh is Godbold Endowed Chair Professor of Electrical and Computer Engineering at Auburn University, USA. Before joining Auburn in 1991, he served on the faculty at the University of Massachusetts in Amherst, and Virginia Tech in Blacksburg. He has held several visiting positions during sabbaticals, including at the University of Tokyo in Japan, the Universities of Freiburg and Potsdam in Germany, the Indian Institutes of Technology, and as Fulbright Awardee at the University Polytechnic of Catalonia in Barcelona, Spain. His technical interests span all aspects of VLSI technology, in particular integrated circuit test and reliability. He has published over two hundred and fifty research papers and holds international patents that have been licensed to industry. He is particularly recognized for his pioneering contributions to statistical methods in test and adaptive testing. He has served as a consultant to many semiconductor, test and EDA companies around the world, including as an expert witness on major patent litigation cases. He has had leadership roles as General Chair/Co-Chair/Program Chair for dozens of international VLSI design and test conferences. Most recently he was Program Co-Chair for the 2014 International Conference on VLSI Design, and Program Chair for the 2015 Asian Test Symposium. He also served on the editorial boards of several journals, including IEEE Design and Test, and on the Steering and Program Committees of many of the major IEEE international test and design automation conferences. He served two terms (2007-11) as Chair of the IEEE Test Technology Technical Council (TTTC), and (2011-15) on the Board of Governors of the IEEE Council on Design Automation (CEDA). Professor Singh is a Life Fellow of IEEE.