1) The Tutorial abstract

This tutorial aims to provide a comprehensive coverage on the analog design flow and the knowledge required for effective analog design.

The tutorial begins with an in-depth exploration of the Process Design Kit (PDK), a fundamental resource for semiconductor design. It covers essential IC components such as resistors, capacitors, and standard cells, along with the analog design flow. The impact of process corners on circuit performance under varying conditions is thoroughly examined, as well as the behavior of IC components in response to process, temperature and voltage fluctuations. Additionally, the tutorial delves into the selection of specific cells from available variants and the importance of choosing suitable components in analog design.

The tutorial then focuses on designing a CMOS-based BGR (Bandgap Reference). A well-designed current source should be immune to temperature and voltage variations, and the BGR circuit serves as an example of this characteristic. Following BGR design, the tutorial extends to the creation of a capless LDO (Low Dropout Regulator) integrated seamlessly with the BGR. The development of low-power protection circuits, including UVLO (Under Voltage Lockout), TSD (Thermal Shutdown), and CFC (Current Foldback Control), is also discussed. These circuits have been designed using SCL's 180nm CMOS PDK in Cadence Virtuoso. Capless LDOs hold significance in System-on-Chip (SOC) designs, particularly in battery-powered low-power devices.

The tutorial proceeds to cover the entire layout design process for the integrated LDO. It discusses critical layout-related considerations, such as matching techniques, latch-up issue resolution, mitigation of concerns like electromigration and antenna effects, and management of well proximity effects. After layout design, the tutorial explores the various checks involved in physical verification, including Design Rule Checks (DRC) and Layout vs. Schematic (LVS) checks. Parasitic extraction, associating each net with resistors and coupling capacitors in the layout, is also explained.

The tutorial further navigates the chip-level layout design, emphasizing the integration of the designed layout with essential I/O pins for external signal interfacing. Post-layout simulations are then explored, covering diverse process corners, voltage levels, and temperature conditions.

Finally, the tutorial culminates with a comprehensive examination of SAR (Successive Approximation Register) ADC (Analog-to-Digital Converter). In summary, this tutorial, titled "Comprehensive Guide to Navigating the Analog Design Landscape: From PDK Foundations to Layout Optimization with Capless LDO and 10-bit SAR ADC Case Studies". It offers a comprehensive journey through the analog design flow, supported by practical design examples featuring BGR, LDO regulators, and SAR ADC.

3) Speaker's biography

a) Arnab Deb: Arnab Deb is currently working with the Secure Hardware and VLSI Design Group at C-DAC Bangalore. His work primarily focuses on various power management analog circuits including BGR, LDO regulator as well as energy harvester combiner topologies such as voltage level detection, power ORing, and inductor sharing. His work on these IPs have been published in various publications. His work on these IPs have been published in various publications. He has presented two of his works at BITS, Pilani for the VDAT conference 2023. One was about a fast transient and low quiescent current capless LDO along with BGR circuit and another on low power protection circuits for linear voltage regulators. He has presented his work on modelling

energy harvesting combiner setups using SPICE in a conference. He has worked at the custom layout design of various analog IPs such as BGR, LDO, SerDes, PLL at TSMC's 45nm technology node. He has also worked for Chipcentre as a part of the SMDP-C2SD program to review the foundry compliance checks for the designs from various academic institutions, making sure that the designs met criteria like clean DRC, LVS, I/O pad size, chip size etc. He has worked extensively on the SCL 180nm Technology node and has contributed significantly to establishing the SCL 180nm Analog/Mixed-Signal tool flow in Cadence Virtuoso. He received his M.Tech in Electronic Design and Technology from Tezpur University, Assam. His research interests includes low power and low TC BGR circuits, PLL, custom layout design of analog circuits.

b) Shramona Roy: Shramona Roy is a Project Engineer working at C-DAC Bangalore for the past two years. She completed her B. Tech and M. Tech in Electronics and Communication Engineering from IIITDM Kancheepuram specializing in VLSI Design. Shramona has been involved in research on Analog and Mixed-Signal circuit designs focusing on low-power applications in the fields of wearable electronics and edge IoT. Her research interests include artificial bio-neurons, neuromorphic encoders, PLL, ADC, and physical security and tamper resistance of sensitive chips. Her work has been published in various conferences and publications. Her paper on a low-power SAR ADC, using a novel RC DAC design, received the Honorable Mention Award at the 27th International Symposium on VLSI Design and Test (VDAT 2023). She is currently involved in the Chips-to-Startup Programme, heading the Analog/Mixed-Signal design team with the main objectives being to indigenously develop custom front-end ASICs and assist various academic institutions in training skilled-manpower in the field. She has worked extensively on the SCL 180nm Technology node and has contributed significantly to establishing the SCL 180nm Analog/Mixed-Signal tool flow.