Title: **The Art of Chip Verification**

Speakers:

P R Sivakumar
Founder and CEO, Maven Silicon
https://www.linkedin.com/in/sivapr/

Putta Satish
Principal Engineer, Maven Silicon
https://www.linkedin.com/in/putta-satish/

Abstract:

The next generation of AI chips demands architectural improvements and new packaging technologies like 2.5D/3D and Chiplets, using newly designed domain-specific CPUs, GPUs, Accelerators, and various IPs and subsystems. Despite the more automation using AI-driven EDA, Verification IPs, methodologies, and technologies, DV engineers need to understand the art of verification for the First-Pass Silicon success.

As per the 2022 Wilson research group functional verification study [Siemens EDA Blog], more than 70% of ASICs require two or more respins, and more than 80% of FPGA projects have non-trivial bugs escaping into production. More than 50% of logic or functional flaws are the leading cause of bugs. It caused more than 70% of FPGA projects and 66% of ASIC projects to be behind schedule. Designing silicon-proven working chips and shipping them on time, meeting the aggressive TTM schedule has always been challenging for the DV engineers. So, in this tutorial, we will explain the art of functional verification using various technologies like simulation, formal and hardware acceleration and prototyping and methodologies like Constrained Random Coverage Driven Verification [CRCDV], Portable Test Stimulus Standard [PSS], exploring IP, Subsystem and SoC verification flows. Also, we will explore how the AI-driven EDA will empower DV engineers to verify the next-gen complex chips efficiently by automating the most time-consuming mundane tasks like simulation debugging.

Tutorial Agenda:

Duration: 3 Hours

1.5 Hours: The Art of Verification
AI-driven Semiconductor Industry
VLSI System Design Overview – IPs, Sub-systems, SoCs, RISC vs CISC, Why RISC-V?
Verification Methodologies Overview – CRCDV – SV & UVM, Code & Functional Coverage, ABV-Formal vs Dynamic, Linting, Emulation, ASIC Prototyping, PSS
Design Verification Challenges and Methodologies – ASIC vs FPGA
AI-driven EDA for DV
Verification IP implementation using UVM.

1 Hour: Case Studies
RISC-V IP Verification Flow
Bluetooth VIP using UVM.
SoC Verification – SoC Verification Environment and Verification Flow

30 Minutes: RISC-V IP Verification using UVM Demo
RISC-V DUT – RTL overview
RISC-V V-Plan, UVM TB architecture and Testcases
Demo: Regression testing, Coverage closure and verification sign-off

Pre-requisite:
Good knowledge/experience in RTL design using any HDL.
Knowledge in RTL verification using Verilog, SystemVerilog and UVM

Target Audience:
Electrical and Electronics UGs and PGs, Experienced ASIC & FPGA RTL designers and verification engineers

Keywords:
VLSI Verification, UVM, SystemVerilog, RISC-V, SoC, VIP, ASIC, FPGA

Bio:

Speaker1:

Sivakumar P R is the Founder and CEO of Maven Silicon. He is responsible for the company's vision, overall strategy, business, and technology. He is also the Founder and CEO of Aceic Design Technologies.

Sivakumar is a seasoned engineering professional who has worked in various fields, including electrical engineering, academia, and semiconductors, for over 25 years. In the semiconductor industry, he has worked as a Verification Consultant for the top EDA companies Cadence, Siemens EDA, and Synopsys, and helped various ASIC and FPGA design houses deploy and use various verification methodologies effectively, resulting in successful tape out of IPs, Chips, and SoCs.

He now specializes in offering Verification IPs and consulting services and EDA flow development, and has delivered corporate training courses for the top EDA and VLSI global MNCs. He is also the author of our online VLSI courses and blogger for Design&Reuse, Semiwiki, and RISC-V Blogs.

He is the recipient of the "Outstanding Technical Achievement" award from Cadence Design Systems and holds a degree in Electrical and Electronics Engineering from Madurai Kamaraj University.

LinkedIn Profile: https://www.linkedin.com/in/sivapr/

Speaker2:

Putta Satish, Principal Engineer at Maven Silicon.

Putta Satish holds an experience of 14+ years in the field of VLSI Verification and Training. He has worked as a verification engineer for various companies like IBM on development of TB for DDR Memory controllers resulting in successful tape out of the chip that was used in IBM's server Z. And also, he worked at Aceic Design Technologies on the development of VIP for Bluetooth Low Energy.

As a trainer at Maven Silicon, he successfully delivered various trainings for New college graduates and corporate trainings on SystemVerilog and UVM at various companies that include World's Largest WiFi MNC Technology Company, World's Largest Mobility Solutions Provider, Leading IP/EDA tool provider company to name a few.

He now specializes in offering training services on RISC-V and ARM architectures and he was trained by ARM on ARM V8A Architecture as Maven Silicon is an ARM Approved Training Partner (AATP)

He is the recipient of the "Outstanding Technical Contribution" award from Aceic Design Systems and holds a Master's degree in VLSI Design from VIT University, Vellore.

LinkedIn Profile: https://www.linkedin.com/in/putta-satish/