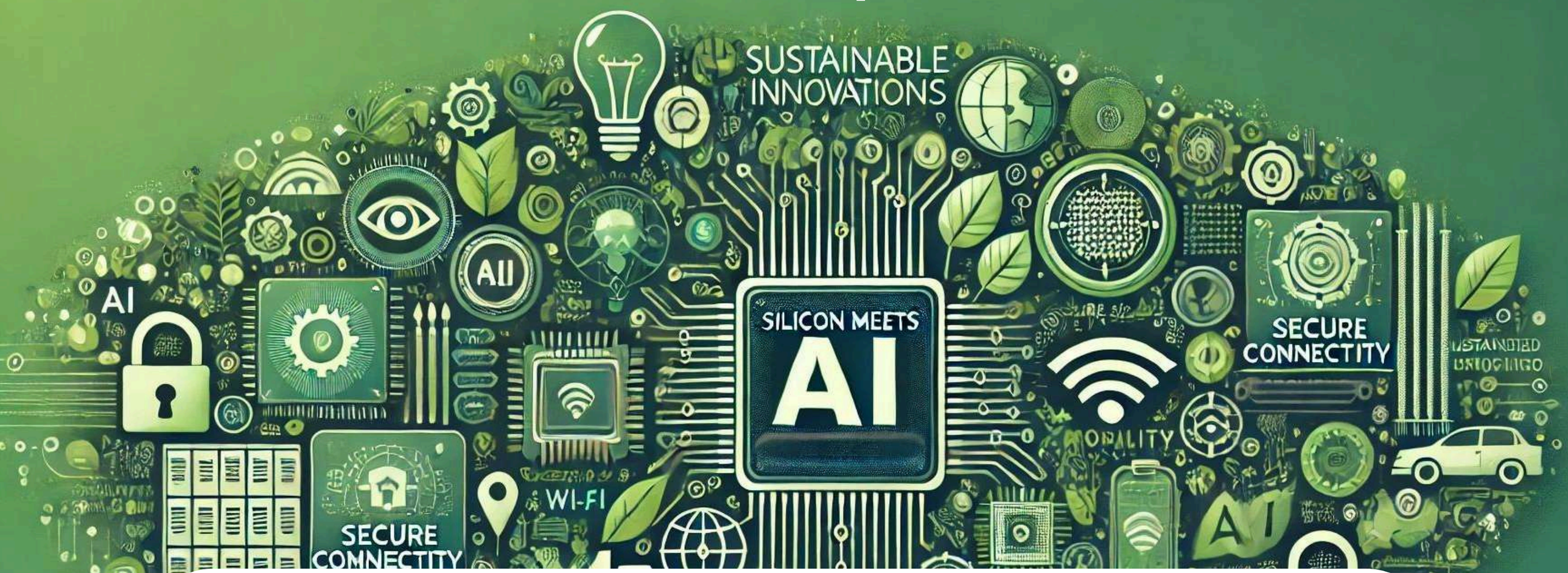
VLSI DESIGN 2025

Embedded System

VLSI Society of India

CALL FOR PAPERS

4-8 JANUARY 2025 | BENGALURU



Silicon Meets AI: Sustainable Innovations in Accelerated Computing, Secure Connectivity, and Intelligent Mobility

TOPICS

- Hardware for Machine Learning and Artificial Intelligence
- Analog & Mixed Signal and, RF Circuits
- Sensors interfacing circuits and systems
- VLSI for Automotive Circuits and Systems
- Test, Verification and Reliability
- Embedded Systems, Internet of Things (IoT), and Cyber-Physical System Design
- Electronic Design Automation
- Low power Digital Systems
- Advances in CAD for VLSI
- Latest trends in device design and modelling
- Chiplets based heterogeneous designs
- Beyond 2D in Packaging and interconnects
- Hardware and Systems Security
- Emerging Memory Technologies
- Advanced process and Material
- Photonic Integrated Circuits & Optical Communication
- Wireless systems 5G and beyond
- Emerging Memory Technologies
- Power & Energy Management
- Emerging Computing & Post-CMOS Technologies
- Quantum Computing
- FPGA Architecture Design – Layout Design, Open FPGA
- Neuromorphic Computing – Spiking Neural Networks, Neuron models

Submissions & Enquiries:
www.vlsid.org

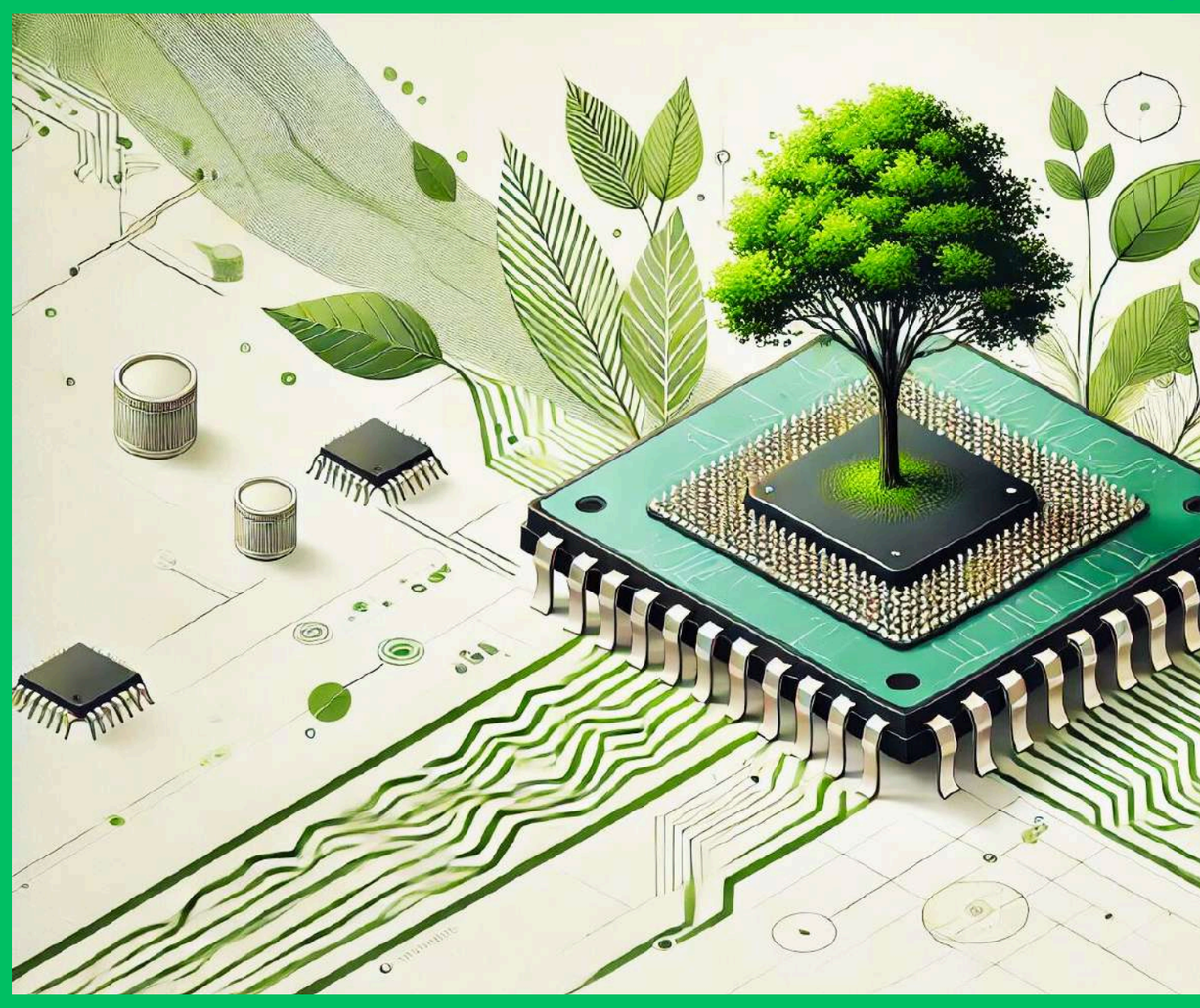
Full Paper Submission Deadline **19th Aug 2024**

Notification for Acceptance **5th October 2024**

CALL FOR PAPERS

Artificial Intelligence (AI) has permeated every facet of our lives. AI advancements through sustainable innovations in accelerated computing, secure connectivity, and intelligent mobility have revolutionized the electronics industry. This evolution has propelled growth across diverse fields of smart automotive, secure homes, healthcare, robust connectivity, and efficient manufacturing.

Within the realm of VLSI and Embedded Systems, the focus has shifted toward accelerated computing, sensing, wireless connectivity, big data, secure connectivity and data conversion. To support this evolution, significant advancement has been observed in EDA/CAD automation, design and manufacturing, and Quantum Computing. Notably, the semiconductor industry remains pivotal in enabling these transformative technologies.



The VLSID 2025 conference provides a platform for researchers and practitioners to explore how VLSI and Embedded Systems can drive disruptive advancements for the next generation.

SUBMISSION GUIDELINES

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Previously published papers or papers currently under review for other conferences/journals should NOT be submitted and will not be considered. Electronic submission in PDF format to the http://www.vlsid.org website is required. Author and contact information (name, affiliation, mailing address, telephone, fax, e-mail) must be entered during the submission process. Paper Format: Submissions should be in camera-ready two-column format, following the IEEE proceedings specifications.

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentations at the conference. Every accepted paper MUST have at least one author registered to the conference by the time the camera-ready paper is submitted; at least one of the authors is also expected to attend the conference and present the paper.

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Hardware for Machine Learning & Artificial Intelligence:

Chips demonstrating system, architecture and circuit innovations for machine learning and artificial intelligence, AI accelerator design, AI boosted circuits and systems for Brain Machine Interface, Intelligent storage, Memory Centric Accelerator Design, Low power autonomous systems, Trusted Architectures for AI. Approximate Computing for AI acceleration. Multiplier Designs for high performance Computing, Activation Functions realization

Test, Verification and Reliability:

Simulation, formal verification, validation at different abstraction levels; All areas of DFT, ATE and BIST for digital designs, analog/mixed-signal IC's, SoC's, and memories, Post-silicon validation and debug; Delay test and speed-binning; Memory test, Reliability and fault tolerance; 2.5D/3D IC testing; Analog and Mixed-signal testing; Static/dynamic defect- and fault-recoverability; Learning-assisted testing; Statistical Testing; Variation-aware design.Hardware and software formal-, assertion-, and simulation-based design verification techniques, Test synthesis and synthesis for testability, Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction, SoC/IP testing strategies Design methodologies dealing with the link between testability and manufacturing, Hardware/software co-verification, Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs), Formal and semi-formal verification and validation techniques, Safety and security in verification and validation, New methods and tools supporting functional safety and security, Self-checking testbenches in analog verification, Any other topics related to design test and verification.

Embedded Systems, IoT, Cyber Physical Systems, Automotive Systems:

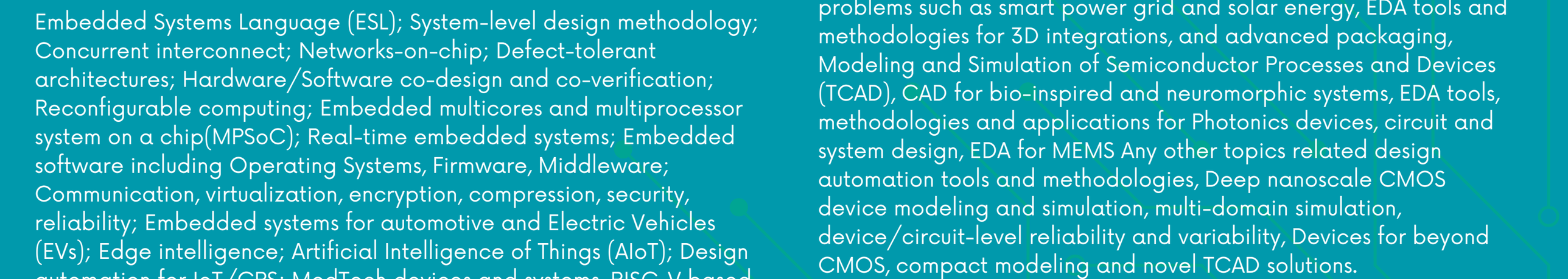
Embedded Systems Language (ESL); System-level design methodology; Concurrent interconnect; Networks-on-chip; Defect-tolerant architectures; Hardware/Software co-design and co-verification; Reconfigurable computing; Embedded multicores and multiprocessor system on a chip(MPSoC); Real-time embedded systems; Embedded software including Operating Systems, Firmware, Middleware; Communication, virtualization, encryption, compression, security, reliability; Embedded systems for automotive and Electric Vehicles (EVs); Edge intelligence; Artificial Intelligence of Things (AIoT); Design automation for IoT/CPS; MedTech devices and systems, RISC-V based systems. Sensor Interfacing, Instrumentation, Biomedical Circuits and Healthcare Systems, Low Noise Circuits, EMI Immune Design, Auto Calibration Techniques, Wearable Electronics, flexible electronics, ultra-low power circuit techniques, circuits, AgriTech Systems, Robotics, and systems for IoT.

Analog & Mixed Signal and RF circuits:

Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; Analog design at lower technology nodes, Analog Circuits for Various Applications, Data Converters, High Speed Interfaces. : RF, mm-Wave and THz transceivers, SoCs, and SiPs. frequency synthesizers, system architecture for 5G and 6G wireless, next generation systems for radar, sensing, and imaging. Reliability aspects in RFICs.

Electronic Design Automation & CAD :

Logic and behavioral synthesis; Logic mapping, simulation and formal verification; Physical design techniques; Post-route optimizations; memory compiler; Simulation tools for design verification; Static Timing Analysis and timing exceptions; Mixed-Signal simulations; EDA for sub-10nm nodes; Design for Debug (DFD) tools; Application of AI/ML in CAD for VLSI; Optimization of Placement and Routing, AI for placement and Routing, CAD for printed circuit boards (PCBs), CAD for secure chips. CAD for bio-inspired and neuromorphic systems. EDA and physical design tools, processes, methodologies, and flows, Design tools for analysis/ tolerance of variation, aging, and soft-errors, Design and maintenance of hard and soft IP blocks, EDA for non-traditional problems such as smart power grid and solar energy, EDA tools and methodologies for 3D integrations, and advanced packaging, Modeling and Simulation of Semiconductor Processes and Devices (TCAD), CAD for bio-inspired and neuromorphic systems, EDA tools, methodologies and applications for Photonics devices, circuit and system design, EDA for MEMS Any other topics related design automation tools and methodologies, Deep nanoscale CMOS device modeling and simulation, multi-domain simulation, device/circuit-level reliability and variability, Devices for beyond CMOS, compact modeling and novel TCAD solutions.



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Power & Energy Management:

Power management and control circuits, regulators; power converter ICs, energy harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators, Power management for automotive systems, battery management circuits and systems.

3DIC, Advanced Packaging, In-Memory & Near-Memory Computing:

Methodologies and tools for Wafer-level packaging, embedded chip packaging, 2.5D/3D integration, Silicon, SiC & Glass interposer, Thermal characterization and simulation, component, system and product level thermal management and characterization, Au/Ag/Cu/Al Wire-bond / Wedge bond technology, Flip-chip & Cu pillar, Solder alternatives, Cu to Cu, wafer-level bonding & die attachment (Pb-free), Fan-out, panel-level, chiplets, SiP, micro-bump, high I/O thermocompression/hybrid bonding, fine-pitch/multi-layer RDL, printable interconnects, Innovative packaging technologies including 3D IC, 2.5D or interposer, and multi-chip module and their impact on system design, Design techniques, methodologies and flows for vertically integrated circuits/chips, Modeling and mitigation of device interactions for 3D ICs, Design of die-to-die interfaces in 3D/2.5D ICs, Design-for-testability and system-level design issues in 3D/2.5D, Die-package co-design, Any other topics related to circuit design, 3D integration and advanced packaging.

Logic and Circuit Design:

Next-generation digital circuits, building blocks, and complete systems (monolithic, 2.5D, and 3D) for reduced power and form factor; Near- and sub-threshold systems; Energy-efficient algorithms and applications; Energy-efficient storage systems; Digital circuits for intra-chip communication; Clock distribution; Low-power and robust design; Digital regulators and digital sensors; Low-power autonomous systems; Low-power communication; Advances in memory architectures for power reduction; Design for low-power FPGA, GPU, NPU and TPU. Circuit design techniques for digital, memory, analog, and mixed-signal systems; Circuit design techniques for high performance and low power; Circuit design techniques for robustness under process variability, electromigration, and radiation; Design techniques for emerging and maturing technologies (MEMS, nano-spintronics, quantum, flexible electronics, multi-gate devices, in-memory computing); Asynchronous circuit design; Signal-processing, graphic-processor, and datapath circuits, Approximate Computing.

Hardware Security:

Secure and trustworthy hardware, Side-channel Attack (SCA), Fault Attacks, and mitigation, Hardware IP Protection, Hardware Trojan attacks and mitigation, Security of IoT/CPS, Firmware and software security, Secure crypto, Automotive security, Physically Unclonable Functions, Hardware Design for Fully Homomorphic encryptions, Security of Trusted Architectures, Polynomial Multipliers, Micro-architectural Security. Attacks and countermeasures including but not limited to side-channel attacks, reverse engineering, tampering, and Trojans, Hardware-based security primitives including PUFs, TRNGs and ciphers, Security, privacy, trust protocols, and trusted information flow, Ensuring trust using untrusted tools, IP, models and manufacturing , Secure hardware architectures Secure memory systems, Post-quantum security primitives, Security challenges and opportunities of emerging nanoscale devices, IoT and cyber-physical system security.

Reconfigurable Computing & Processor Design:

Autonomous/adaptable/reconfigurable systems and architectures, FPGA Accelerator Design, Placement & Routing of FPGA layout, High-performance, energy-efficient multi-core and many-core (heterogeneous) processor architectures. Microarchitecture design techniques for single-threaded and multi/many-core processors, such as instruction-level parallelism, pipelining, caches, branch prediction, multithreading, and networks-on-chip; Techniques for low-power, secure, and reliable processor architectures; Hardware acceleration for emerging applications including NVM, quantum, neuromorphic, bio-inspired; Hardware support for processor virtualization; Real-life design challenges: case studies, tradeoffs, retrospectives, HW/SW prototyping and emulation on FPGAs, Application driven heterogeneous computing platforms, Chiplets based Heterogeneous system design.

Quantum Computing & Neuromorphic Computing:

Cryogenics electronics for processors & sensors. Control & Readout quantum systems, Quantum Information processing systems, Quantum logic circuits, Quantum algorithms, spin-based computing, reversible computing, approximate and stochastic computing.

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