Overview

4th Jan - T1
5th Jan - T2
6th Jan - C1
7th Jan - C2
8th Jan - C3

Sheet 1: *4th Jan - T1*

Start	End	Duration	4th January, 2025 - Saturday			
8:00 AM	9:00 AM	1:00	Registration			
9:00 AM	9:30 AM	0:30	Tutorial Inauguration: Navin Bishnoi, Srikanth Settikere, Rajeev Shrivastava, Gaurav Goel, Prof. Santosh Kumar Vishvakarma, Anupam Chattopadhyay, Sumit Goswami			
			Grand Ball Room (First floor)	**Royal Ball Room (First floor)**	**Turret (First floor)**	**Maharaja (Ground floor)**
			Track Chair: Gaurav Goel	**Track Chair: Santosh Vishvakarma**	**Track Chair: Anupam Chattopadhyay**	**Track Chair: Sumit Goswami**
9:30 AM	11:00 AM	1:30	Multi-Stacked More-than-Moore Emerging Devices by Prof Sudeb Dasgupta, IIT Roorkee	Large Language Models (LLM) for Hardware Verification by Chandan Kumar Jha, University of Bremen	Electronic Design Automation for Fully Homomorphic Encryption based Privacy Enabled Computing by Debdeep Mukhopadhyay, IIT KGP	Design Flow from VLSI-Algo to ASIC-Chip Fabrication of Hardware-Efficient Spectrum Sensors for Dynamic Spectrum Access by Rahul Shrestha, IIT Mandi
11:00 AM	11:30 AM	0:30	Tea Break			
11:30 AM	1:00 PM	1:30	HSIO Link– SERDES Design, Analysis and Adaptive Equalization Techniques by Ranjan Sahoo, NXP	Challenges and Opportunities of Applying AI/ML in VLSI Design Workflows by Arpan Sircar, Intel	Hardware Security with Logic Locking by Jai Gopal Pandey, CEERI Pilani	Domain Specific Accelerator (DSA) Architectures for Signal Processing, Communications, and Machine Learning by Kiran Gunnam, Micron
1:00 PM	2:00 PM	1:00	Lunch Break			
2:00 PM	3:30 PM	1:30	Industry-Driven Formal Verification: Techniques for Modern VLSI Design by Achutha Kirankumar, Synopsys	Resistive Switching Memory: The Major Challenges and IP Design prospectives by Writam Banerjee, Globalfoundries	Cognitive Systems and Materials: Part 1 by Farhad Merchant, Groningen University	Embedded Systems and Internet-of-Bodies I by Venugopal Vishwanath, Renesas
3:30 PM	4:00 PM	0:30	Tea Break			
4:00 PM	5:30 PM	1:30	Advancements in CPU Verification by Suraj Kamat, ARM	Insights into memory technologies and introduction to latest DRAM devices by Shyam Sharma, Cadence	Cognitive Systems and Materials: Part 2 by Tamalika Banerjee, Groningen University	Circuits and Systems for Ultra-low-Power and Secure HBC for Next-gen of Intelligent Wearables and Implants by Shreyas Sen, Purdue University

Sheet 2: *5th Jan - T2*

Start	End	Duration	5th January, 2025 - Sunday			
8:00 AM	9:30 AM	1:30	Registration			
			Grand Ball Room (First floor)	**Royal Ball Room (First floor)**	**Turret (First floor)**	**Maharaja (Ground floor)**

			Track Chair: Gaurav Goel	**Track Chair: Santosh Vishvakarma**	**Track Chair: Anupam Chattopadhyay**	**Track Chair: Sumit Goswami**
9:30 AM	11:00 AM	1:30	Introduction to AI Inferencing Hardware by Preetham Lobo, IBM	Introduction to Emulation, Modelling and Verification Acceleration by Gaurav Garg, Marvell	Systematic Design of Voltage Regulators for Mixed Signal Applications by Rakesh Kumar Palani, IIT Delhi	Leaky ML: Physical Attacks on Edge-based Machine Learning (EdgeML) Accelerators by Shivam Bhasin, NTU Singapore
11:00 AM	11:30 AM	0:30	Tea Break			
11:30 AM	1:00 PM	1:30	Application-Specific AI Inference Chip: 90-Min Hands-On by Raja Gopal Hari Vijay, Zoho Journey from Idea to Implementation Using Open Source for Resource-Constrained Systems	Digital Circuit Testing and Testability by Indranil Sengupta, IIT KGP	Self-Adaptive Control Techniques for Voltage Regulators – A simplified AI for power management with least data processing by Qadeer Ahmad Khan, IIT Madras	Optimized Edge Intelligence with Compute-in-Memory: Bridging Circuits, Architectures, and AI Workloads by Amit Ranjan Trivedi, Univ of Illinois Chicago
1:00 PM	2:00 PM	1:00	Lunch Break			
2:00 PM	3:30 PM	1:30	Advanced GaN Compact Modeling for Efficient RF Power Amplifier Design by Yogesh Chauhan, IIT Kanpur	Primer on Data in Quantum Machine Learning by Aviral Shrivastava, Arizona State University	RISC-V: A Comprehensive Guide to Architecture, Design, and Implementation by Amlan Chakrabarti, University of Calcutta	On-Chip ESD Design: Complexity in Simplicity by Nathaniel (Nate) Peachey, ESD Association
3:30 PM	4:00 PM	0:30	Tea Break			
4:00 PM	5:30 PM	1:30	Introduction to Silicon Photonics: Current Status and Future Trends by Mukesh Kumar, IIT Indore	Solving Combinatorial Optimization Problems with a Quantum Computer – the Qiskit pattern approach by Ritajit Majumdar, IBM	Scalable system simulations for RISC-V architectures and performance analysis for machine learning workloads by Erwan Lenormand, IMEC	Introduction to IC Packaging by Raghavendra Anjanappa, Tata Electronics

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Sheet 3: *6th Jan - C1*

Start	End	Duration	6 January, 2025 - Monday
8:00 AM	8:45 AM	0:45	Registration
8:45 AM	9:00 AM	0:15	Welcome
9:00 AM	9:10 AM	0:10	Inauguration & Lamp Lighting Welcome Dignitaries on the stage: Chitra Hariharan, VLSI Society of India Shri Ashwini Vaishnaw, Hon'ble Minister of Railways, I&B, Electronics & IT Dr. Chris Miller, Author of "CHIP WAR" Book Shri Tejasvi Surya, Member of Parliament Patrick Johnson, SVP, Microchip Technology Sandeep Bharathi, CDO, Marvell Technology Hitesh Garg, VP & Country Head, NXP Semiconductors Prof. Vishwani Agrawal, Auburn University Dr. Satya Gupta, President, VLSI Society of India
9:10 AM	9:20 AM	0:10	VLSID-2025 Conference Highlights - Srikanth Settikere, VP, Microchip Technology & Prof. Madhav Rao, IIIT Bangalore
9:20 AM	9:30 AM	0:10	VLSI Society of India (VSI) Key Announcements & Plans - Dr. Satya Gupta, VLSI Society of India
9:30 AM	10:00 AM	0:30	"Chip-Pe-Charcha": Shri Ashwini Vaishnaw & Dr. Chris Miller, Moderated by - Dr. Satya Gupta

10:00 AM	10:30 AM	0:30	Keynote: "Accelerating the AI infrastructure" Noam Mizrahi, EVP & Corporate CTO, Marvell Technology						
10:30 AM	11:00 AM	0:30	Keynote: "Bringing AI into Silicon and Systems for a safe and secure AI (Automotive/Industrial IoT) World!" Venu Puvvada, SVP, NXP Semiconductors						
11:00 AM	11:30 AM	0:30	Exhibits Inaguration & Tea Break						
11:30 AM	12:00 PM	0:30	Keynote : "Intelligence and accelerated computing for smart , connected and secure systems" Patrick Johnson, SVP, Microchip						
12:00 PM	12:25 PM	0:25	Keynote : "Building the Semi-conductor Eco System & Empowering the Design Innovation in INDIA" Murty Dasaka, VP – Head of PDK-Design Enablement & Design Services, TEPL						
12:25 PM	12:50 PM	0:25	Keynote : "Reimagining Semiconductor Design with AI Optimized EDA" Shankar Krishnamoorthy, Head of Technology and Product Development Group, Corporate Staff, Synopsys						
12:50 PM	2:00 PM	1:10	Lunch Break						
2:00 PM	2:25 PM	0:25	Keynote : "India's Semiconductor Future: Harnessing Innovation. R&D, Local Demand, Talent and Manufacturing for Global Leadership" Jasbir Singh Gujral, MD, Syrma SGS						
2:25 PM	2:45 PM	0:20	Keynote : "Shaping the Next G in Wireless Communication" Dr. Naveen Yanduru, VP, Renesas Electronics/ CG Power						
2:45 PM	3:40 PM	0:55	Panel Discussion - "Fabless Landscape: Scaling up Domestic and Global Companies in India" Anurag Gupta - Alphawave, Kripa Venkatachalam - Cadence, Jayakumar Parasuraman - Nvidia, Siva Raghu Ram Voleti - Moschip, Mukesh chopra - ST Microelectronics Moderator - Sumit Goswami - Qualcomm						
3:40 PM	4:10 PM	0:30	Tea Break						
			Royal Ball Room (First floor)	**Diya (First floor)**	**Turret (First floor)**	**Grand Ball Room (First floor)**	**Jamwar (Ground floor)**	**Maharaja (Ground floor)**	**Maharaja (Ground floor)**
			Track : Test, Verification and Reliability Session chair- Jaidev Shenoy	**Track : Embedded Systems Session chair- Neha Srivastava**	**Track : AIML Hardware Accelerators Session chair- Viveka K R**	**Track: Industry Forum Session chair: Biswajit Patra**	**Track: Design Contest Sesson chair: Nanditha Rao**	**Track: User Design Track Session chair: Srobana Mitra**	**Poster Session, Session Chair - Sakshi Arora**
4:10 PM	4:30 PM	0:20	Invited Talk on "Formal verification of large integer multipliers" by Masahiro Fujita	PaperID: 351, Title - An efficient RISC-V Vector Coprocessor for Heart Rate Variability Detection on Edge, Authors - Uday Kiran Pedada, Tarun Sharma, Deepank Grover and Sujay Deb	Invited Talk on "Herding Llamas: An infrastructure silicon perspective" by Harish Dixit , Dheepak Jayaraman	Industry Forum - Advancements in Optical Chip Design: Transforming Data Center Networks, Kishore Kota, Marvell	Microchip : Hardware Software Co-Design of Multi Receiver Narrowband Spectrum Sensing for Cognitive Radio using Deep Learning : Sardar Vallabhbhai National Institute of Technology Securing and Accelerating Vehicle-to-Vehicle Communications to combat Cyber-Threats and enabling ML-Based intelligent decision in Autonomous Vehicles : Indian Institute of Technology - Patna A Dual-Mode Assistive and Therapeutic Device for Enhanced Hand Mobility Using Myoware Sensors and Soft Robotics : International Institute of Information Technology - Bangalore Project Insight : Kumaraguru College of Technology AI Driven Retail Automation : IIIT - Kottayam NXP: Hey Auxi!!: Your All-	ID 8: Scalable JTAG solution for 2.5D Multi-die Design; Amit Wangoo, Ramu Setty, Subhra Lahiri and Amit Wangoo ID 16: Automated analog checkers/assertion based methodology for pre- silicon verification in mixed signal SoC; Aadhar Sharma, Avinash Chaudhary, Bhavya Shah and Saurabh Kandpal (b-shah@ti.com) ID 18: DM-crypt solution based on OP-TEE; Sahil Malhotra and Pankaj Gupta ID 25: Dynamic Reconfiguration in Embedded Systems; Ashish Kumar and Sandeep Naduvalamane ID 61: Hardware Implementation of AI/ML based Target Identification; Usha Mehta, Vaishali Dhare, Aryan J. Shah and Mantra Solanki ID 67: Scalable and Secure PECVD SiO2-Based OTP Memory with Differential PUF Implementation; Shreeniwas Daulatabad, Shreyas Deshmukh,	PaperID: 208, Title - Advancing Neural Network Performance with Probabilistic Computing for ReLU Function, Authors - Srinivasu bodapati, AMIT SINGH and Amit Kumar Jangid. PaperID: 310, Title - MAGIC-based High-Speed Adders for In-Memory Computing using Memristors, Authors - Srinivasu bodapati and Shri Janani Senthil. PaperID: 113, Title - FRoZN: Fault-Tolerant Routing Technique using Reinforcement Learning for ZMesh NoC, Authors - JITESH CHOUDHARY, Imran Hussain Barbhuiya, Dharrun Singh M and Dr. Soumya J. PaperID: 377, Title - QuaLITi: Quantum Machine Learning Hardware Selection for Inferencing with Top-Tier Performance, Authors - Koustubh Phalak and Swaroop Ghosh. PaperID: 127, Title - Low Form-Factor Switchless Dual-Band Matching Network for RF Power Harvesting Systems, Authors - Arun Mohan, Saroj Mondal, Yash Nageshwar Rayudu and Roy P. Paily.
4:30 PM	4:50 PM	0:20	PaperID: 118, Title - PrOFraC: Property Ordering and Frame Clause Reuse for Multi-Property Verification, Authors - Sourav Das, Aritra Hazra, Pallab Dasgupta, Himanshu Jain and Sudipta Kundu	PaperID: 326, Title - Advancing Rehabilitation through Low Weight Hand Assistive System: Design and Impact Analysis, Authors - Kushagra Singh, Kafil Abbas Momin, Anshul V. Patil and Madhav Rao	PaperID: 172, Title- A 14-nm Energy-Efficient and Reconfigurable Analog Current-Domain In-Memory Compute SRAM Accelerator, Authors- Aya Amer, Maitreyi Ashok, Xin Zhang, John Cohn and Anantha P. Chandrakasan	Industry Forum - Software Defined Vehicle (SDV), Rahul Bedi, NXP			

							in-One Interactive Home Companion : Amrita School of Engineering MoodSync: Emotion-Based Music/Visual Effects Recommendation through Wearables : International Institute of Information Technology Museum Guide Robot with RFID-Based Artifact Detection and Sign Language Support : Rajiv Gandhi University of Knowledge Tec e-SAM (Electronic Secure Asset Management) : RV College of Engineering YOG GURU - AI-Integrated Smart Yoga Device for Personalized Yoga Experience : Thapar University Texas Instruments : Body Vitals Extraction : IIT - Indore Warehouse Management System using Autonomous Robots and Centralized Coordinator : International Institute of Information Technology, Bangalore Hardware Implementation of Video Violence Recognition and Women Tracking based Surveillance System using Machine Learning : M S Ramaiah University of Applied Science Real Time LLVE : National Institute of Technology Karnataka, Surathkal Helmet detection : National Institute of Technology, Manipur	Shatadal Chatterjee, Abhishek Kadam and Udayan Ganguly ID 71: Application of Machine Learning Models for SoC Level Mixed-Signal Verification: Learnings, Challenges and Opportunities; Lakshmanan Balasubramanian, Sooraj Sekhar, Ankush Ankush, Venkateswaran Padmanabhan, Bama Srinivasan, Ranjani Parthasarathi, Selvi Ravindran, Dhurga Devi J and Ramakrishna P V	PaperID: 370, Title - OwlsEye: Real-Time Low-Light Video Instance Segmentation on Edge and Exploration of Fixed-Posit Quantization, Authors - Gaurav M. Shah, Abhinav Goud, Zaqi Momin and Joycee Mekie. PaperID: 151, Title - A Tug-of-War between Static and Dynamic Memory in Intel SGX, Authors - Sandeep Kumar, Abhisek Panda, Advait Nerlikar and Smruti R. Sarangi. PaperID: 175, Title - RISC-V Based Secure Processor Architecture for Return Address Protection, Authors - Lalit Sharma and Neeraj Goel. PaperID: 146, Title - Optimal Respiratory Rate Estimation with mmWave Sensing using PYNQ System-on-Chip Platform, Authors - Mohammed Musayyeb Sherwani, Mohammad Abdul Azeem, Mohd Usman, SIDDIQUE AHMAD, Mujeev Khan, Raaziyah Shamim and Mohd Wajid. PaperID: 258, Title - A 0.27-THz Frequency Multiplier Chain using Harmonic Mixing with Multiplication of ×18 in 65-nm CMOS, Authors - Shiva Bollam Prasad and Mahima Arrawatia. PaperID: 66, Title - Boosting System-on-Chip Performance through AI-assisted Optimization using Compositional Neural Networks, Authors - Surinder Sood and Priyatam Roy. PaperID: 273, Title -AI-Driven Anomaly Detection in Oscilloscope Images for Post-Silicon Validation, Authors - Kowshic Ahmed Akash, Tobias Wulf, Torsten Valentin, Alexander Geist, Ulf Kulau and Sohan Lal. PaperID: 229, Title - A Constructive High-Speed Crypto-mining Approach with Dual SHA-256 on an FPGA, Authors - Velamala Pavan Kumar and Aravindhan Alagarsamy. PaperID: 236, Title - Enhancing Digital Microfluidic Biochip Operations with Scheduling Interval Method, Authors - Nirmala N and Dr GRACIA Nirmala Rani D. PaperID: 209, Title - A First Principle Based Comparative Study Between Pristine and Au-modified Graphene Nanosheet towards Acetaldehyde Sensing Performance, Authors - Indranil Maity, Soubarno Chatterjee and Souvik Bhanja.
4:50 PM	5:10 PM	0:20	PaperID: 185, Title- Robust Verification Methodology for Scan Chain in Memories, Authors - Rajat Kohli, Umang Deep, Vaishnavi Holla and Jwalant Mishra	PaperID: 91, Title - hbcLock: Encrypted RF Communication Utilizing Body-Coupled Keys for the Internet of Bodies, Authors - Soumick Majumdar, Anshul Madurwar, Anmol Shetty and Kurian Polachan	PaperID: 279, Title - Accelerating U-Net: A Patchwise Memory Optimization Approach for Image Segmentation, Authors- MODIBOYINA CHAITANYA, Syam Babu Gundumilli, Soumya Kanti Ghosh and Indrajit Chakrabarti	Industry Forum - Microcontroller in Edge Computing, Choudhary Musunuri, Microchip			
5:10 PM	5:30 PM	0:20	PaperID: 217, Title- Advancing Functional Safety: Improving Failure Mode Analysis and Fault Injection Using Automation and GNN Algorithms, Authors - Amurt Prakash, Abhijeet Singh, Pooja Madhusoodhanan, Padma Arvind and Prasanth Viswanathan Pillai	PaperID: 12, Title- TIPANGLE: Traffic Tracking at City Scale by Pose Estimation of Pan and Tilt Traffic Cameras on Edge Devices, Authors- Shreehari Jagadeesha, Edward Andert and Aviral Shrivastava	PaperID: 313, Title- LAMA: A Latency Minimum Resource Constraint Accelerator for CNN Models, Authors- Sutirtha Bhattacharyya, Maddala Karthik, E Bhawani Eswar Reddy, Fedrick Nongpoh and Chandan Karfa	Industry Forum - Pioneering India's AI Future, Biswajit Patra, Krutrim			

									Invited Poster 1, Title - ESD Electronic Design Automation Challenges - New Revision of ESDA Technical Report ESD TR18.0-01 , Authors - Subhadeep Ghosh, Nate Peachey, Souvick Mitra.

Sheet 4: *7th Jan - C2*

Start	End	Duration	7 January, 2025 - Tuesday
8:00 AM	9:15 AM	1:15	Registration
9:15 AM	9:30 AM	0:15	Welcome & Recap of Day 1
9:30 AM	9:50 AM	0:20	Keynote : "Leading AI @ the Edge" Sundarrajan Subramanian, VP, Qualcomm
9:50 AM	10:10 AM	0:20	Keynote : "Enabling Intelligence Through Sustainable Computing" Ankur Gupta, VP & GM, Siemens EDA
10:10 AM	10:30 AM	0:20	Keynote : "Emerging Trends in Semiconductor Downstream Industry" Raghu Panicker, CEO, Kaynes Semicon
10:30 AM	11:00 AM	0:30	Fireside Chat : "Electronics & Semiconductors, Driving Mission Viksit Bharat-2047" Santhosh Kumar - MD, Texas Instruments, Sanjay Nayak - Co-Founder, Tejas Networks, Ganapathy Subramaniam - Managing Partner, Yali Capital
11:00 AM	11:30 AM	0:30	Tea Break
11:30 AM	11:50 AM	0:20	Keynote : "Chiplets: The new frontier for the semiconductor industry" Sundeep Gupta, MD India & VP CR&D Engineering, Alphawave Semi
11:50 AM	12:10 PM	0:20	Keynote : "Moore's Law, Advanced Packaging and Heterogeneous Integration - Do they hold the key for enabling Future Systems?" Prof. Madhavan Swaminathan, Penn State University
12:10 PM	12:30 PM	0:20	Keynote : "Futureproofing Indian Semiconductor Design Capability: A SWOT Analysis" Sumedha Limaye, VP, Quest Global
12:30 PM	12:50 PM	0:20	Keynote : "The Future of Hardware Technologies for Computing" Prof. Subhasish Mitra, Stanford University
12:50 PM	1:50 PM	1:00	Lunch Break
1:50 PM	2:35 PM	0:45	Panel Discussion : "Building India as a product Nation: Serving the Domestic Market and Applications" Akshat Jain - Marvell, Dennis J. - Syrma SGS, Srikanth Puvvada - Krutrim, Amardeep Punhani - NXP, Satyabodh Kadni - MediaTek Moderator: Prof. Manoj Choudhary - Vice Chancellor, Gati Shakti Vishwavidyalaya

			Royal Ball Room (First floor)	Diya (First floor)	Turret (First floor)	Grand Ball Room (First floor)	Maharaja (Ground floor)	Jamavar (Ground floor)	Maharaja (Ground floor)
			Track : Analog & Mixed Signal Design Session chair- Sanjay Wadhwa	**Track: Embedded Systems Session chair- Neha Srivastava**	**Track: Hardware Security Session chair- Utsav Banerjee**	**Track: Industry Forum, WiE Session Chairs - Prasad Joshi, Rashna Seli**	**Track : User Design Track Session chair - Ulhas K**	**Track : PhD Forum Session Chair - Ruchika Gupta**	**Posters Day 2 Session chairs- Priyesh Shukla**
2:35 PM	2:55 PM	0:20	PaperID: 178, Title -Pin Efficient Tri-Level based Inductive Coupling Transceiver for 3D ICs, Authors- Soumojit Bakshi, V K Surya and Nijwm Wary	Invited Talk on "Memory Climbs Higher – 3D Stacking and Thermal Awareness" by Preeti Ranjan Panda	Invited Talk on "Securing Hardware for Designing Trustworthy Systems" by Prabhat Mishra	Industry Forum - Evolving Indian semi market landscape and what TEPL is targeting, Jnaneshwar Madugonda, Dr. Charan Gurumurthy, Tata Electronics Pvt Ltd	ID 27: VLSID_UDT_Novel Methodology for PreSilicon HTOL estimation and Reliability qualification; Mathangi Raghuraman and Utkarsh Srivastava	PhD Forum PID-2 : Automated Security Assessment for Fault Injection Attacks and Improper Realizations of Embedded Crypto Software; KEERTHI K (Indian Institute of	PaperID: 284, Title - Optimizing Multipliers: An Energy-Efficient Design Using a Novel 3:2 Compressor, Authors - L Hemanth Krishna, Sreehari Veeramachaneni, srinivasu bodapati, Bhaskara Rao Jammu and Noor Mahammad Sk. PaperID: 232, Title - Meta-

							ID 35: Machine Learning Augmented Precise Memory Yield Estimation Using Sensitivity Based Design Partitioning Approach; Ashish Kumar, Shashank Gupta and Rakesh Shenoy ID 40: Automated Routing Corridors using Python (AutoPyRoute); Anmol Khatri and Lalit Arora ID 52: Additional Pessimism Removal in Static Timing Analysis; Aryan Garg, Prabhat Kumar Maurya, Manish Verma, Hemlata Gupta and Kerim Kalafala ID 59: SACF – Synthesis Auto Convergence Flow; Bharat Goyal, Pardhu Pavan and Subbash K P ID 12: Cross-die timing methodology for Next-Gen Chiplet SOCs; Animesh Sharma, Deepon Saha, Animesh Jain, Aniket bharat Waghide, Dhruvin Shah and Rajesh Anand	Technology Madras) PID-10 :Efficient Reduction of Resources and Noise in Discrete Quantum Computing Circuits; Ritajit Majumdar (IBM Quantum, IBM India Research Lab) PID-16 : Efficient VLSI-Architectures and ASIC-Fabrication of Channel Decoder for Contemporary Wireless-Communication Systems; Anuj Verma, Rahul Shrestha (Indian Institute of Technology Mandi) PID-35 : A Battery-less Energy Harvesting Front-end for Powering Multiple IoT Nodes; Aditi Chakraborty, Ashis Maity (Indian Institute of Technology Kharagpur) PID-47 : Design and Analysis of Energy-Efficient Sram Based On-Chip In-Memory Computation for Machine Learning Applications; Prasanna Kumar Saragada (ST Microelectronics), BISHNU PRASAD DAS (IIT Roorkee) PID-76 : CMOS mm-Wave Broadband Transmitter for 5G Applications; Anik Batabyal (Silicon Labs)	Heuristic Optimization of Custom Heterogeneous Blocks Defined eFPGA Design, Authors - Bhargav D V, Pradyumna G and Madhav Rao. PaperID: 134, Title - An Innovative Solution to Improve Ultra Low Voltage Writability and Leakage in GPU SRAMs, Authors - Deepesh Gujjar, Sanatkumar upadhye, Sandipan Sinha, Taha Khursheed, Jigar Patel, Manish Trivedi and Sagar abachi. PaperID: 14, Title -Bidirectional Spiking Neuron Based Dual-Mode Signal Acquisition Front-End System, Authors - Tamal Chowdhury and Pradip Mandal. PaperID: 262, Title -Hardware Implementation of Blind Decoding of Downlink Control Information for 5G, Authors - Anu rajarajeswari Y, Nitin Chandrachoodan, Anji Babu Vadapalli and Klutto Milleth J. PaperID: 186, Title - Low-Power and Superior Performance Design of Ternary Logic Cells Using CNFET and MOSFET Devices for VLSI Applications, Authors - Siva Chinmai Varma Bhupathiraju, Sai Krishna Sridhara, Yashwanth Komuravelly and Ramakant Yadav. PaperID: 282, Title - Design of Manchester Carry Chain Hybrid Adder for MASH 1-1-1 Delta Sigma Modulator for Fractional-N Frequency Synthesizers, Authors - ABHINAV S, Karthikeya Busam, Ishan Acharyya, Anushka Tripathi and Abhishek Srivastava. PaperID: 196, Title - Enhancing Reliability and Energy Efficiency in Network-on-Chip Architectures through Hybrid Sorting Algorithm-Based Core Mapping, Authors - B Naresh Kumar Reddy, Srinivasulu Jogi and Charan Krishna. PaperID: 378, Title - A Early Bug Detector – A Verification Methodology for DFD-SOC RTL Parameters, Authors - Bhagyalakshmi C, Madhav Lekkala and Maneesh Pandey. PaperID: 120, Title - TimeFloats: Train-in-Memory with Time-Domain Floating-Point Scalar Products, Authors - Maeesha BinteHashem, Benjamin Parpillon, Divake Kumar, Dinithi Jayasuria and Amit Ranjan Trivedi. PaperID: 345, Title - Layer-Specific Hardware Pooling Designs for CNN Accelerators, Authors - Vinay R, Mahati Basavaraju and Madhav Rao. PaperID: 126, Title - Effective Memory Management and Sparse Aware Cache for Row-wise Sparse CNNs, Authors - Balasubramaniam MC, Basava Naga Girish Koneru and Nitin Chandrachoodan. PaperID: 191, Title - An Ensemble MLP-RF Model for the Prediction of DG-MOSFETs: Addressing Fabrication Process Variations, Authors - M. Vaikunth, Khushwant Sehra,
2:55 PM	3:15 PM	0:20	PaperID: 238, Title - N-Well Patterning of p-type CMOS Substrate for Improving Quality Factor of On-Chip Inductors at Millimeter-Wave Frequencies, Authors - Subbareddy Chavva and Immanuel Raja	PaperID:: 156, Title - Multi-Object Detection through Meta-Training in Resource-Constrained UAV-based Surveillance Applications, Authors - Abhishek Yadav, Vyom Gupta, Kethireddy Harshith Reddy, Masahiro Fujita and Binod Kumar	PaperID: 162, Title - TRANSPOSE: Circuit Transformations for Power Side-Channel Security at Register Transfer Level, Authors- Nilotpola Sarma, Anuj Singh Thakur and Chandan Karfa				
3:15 PM	3:35 PM	0:20	PaperID: 153, Title- Analysis and Design Considerations for MASH of Noise Shaped SAR ADCs, Authors- Arundeepakvel R and Ankesh Jain	PaperID: 204, Title-MERGERS: Multi-access Edge Resource GovErnance for Real-Time SaaS Systems, Authors- Aakashjit Bhattacharya, Arnab Sarkar and Ansuman Banerjee	PaperID: 92, Title - ABMF: Adaptive Bonsai Merkle Forests for efficient integrity verification in secure persistent memories, Authors - Kartikay Bhardwaj and Hemangee Kapoor				
3:35 PM	3:55 PM	0:20	PaperID: 167, Title - A 0.5pJ/bit 7.2Gbps HBM3 PHY on Intel4 with EMIB Packaging and Unmatched Receiver Architecture on PHY side with Per Bit Deskew Correction, Authors- Aakash Hasmukhray Mehta, Mohammad m. Rashid, Aruna kumar Lakya Srinivasamurthy, Sampath Dakshinamurthy, Javed S. Gaggatur, Anil Kumar Goyal, subbu manam, Harshit Gupta, sandeep sukumar, vipin k. mishra, Koushik n. s, santosh nekkanti, Sambaran Mitra, Pooja K. Jadhav, M Chandra Shekar, dudekula humayun, Michael C. Rifani, Jianyong Xie and Andrew P. Collins	PaperID: 353, Title-LO-SC: Local-only Split Computing for Accurate Deep Learning on Edge Devices, Authors - Luigi Capogrosso, Enrico Fraccaroli, Marco Cristani, Franco Fummi and Samarjit Chakraborty	PaperID: 306, Title - True-PolyTronik: Securing Circuits Against Laser Logic State Imaging Attack Using RFET, Authors - Sajjad Parvin, Chandan Kumar Jha, Frank Sill Torres and Rolf Drechsler	Opening remarks by Rashna Seli Zaroo (IESA-WiSE CiG) WiE-Fireside. Covering inspiring career journeys: Malini Narayanamoorthi (Renesas) Moderator: Anuja			

									Vandana Kumari and Manoj Saxena. PaperID: 382, Title - HapticGuide: Interactive Wearable Braille Guide for Enhancing Visual Education, Authors - Divyansh Singhal, Yash Gupta, Daksh Sharma, Chinmay Sultania and Madhav Rao. PaperID: 331, Title - TCAD based Study of String Current Variability in 3D NAND Flash Memory, Authors - Mrinmoy Mahapatra, Prathamesh Ganesh Kekarjawlekar and Dr. Akshay K. Invited Poster 2, Title - ESD Technology Roadmap, Authors - Nate Peachey, Subhadeep Ghosh, Souvick Mitra.
3:55 PM	4:15 PM	0:20	Tea Break						Tea Break
			Royal Ball Room (First floor)	**Diya (First floor)**	**Turret (First floor)**	**Grand Ball Room (First floor)**	**Maharaja (Ground floor)**	**Jamavar (Ground floor)**	**Maharaja (Ground floor)**
			Track: EDA & CAD Session chair- Chandan Karfa	**Track: Processors and Reconfigurable Computing Session chairs- Nanditha Rao & Madhura Poornaprajna**	**Track: Logic and Circuit Design Session chair- Sparsh Mittal**	**Track: Industry Forum, WiE Session Chairs - Prasad Joshi, Rashna Seli**	**Track : User Design Track & Papers - Power Management, Session Chairs - Spandana R, Qadeer Khan**	**Track : Student Research Forum Session chairs - John Jose, N Venkatesh, Sridhar Kaip**	**Posters Day 2**
4:15 PM	4:35 PM	0:20	PaperID: 59, Title- Physical Synthesis Optimization Prediction using Machine Learning, Authors - Sourav Saha, Anmol Khatri, Lalit Arora, Raj Yadav and Rakshit Bazaz	PaperID: 215, Title - Lichen: Leveraging Coupled Heterogeneity, Authors - Prakhar Diwan, Nirmal Kumar Boran and Virendra Singh	PaperID: 277, Title - PAF-Enc: Position Affine Encoding to reduce bit-flips in Non-Volatile Main Memories, Authors - Swati Upadhyay and Hemangee Kapoor	WiE-Invited talk : Rituparna Mandal (synopsys)	ID 66: Achieving Superior Jitter Performance and Power Efficiency of CMOS Clock Delivery over 50mm routing channel at SoC in 2nm GAA Technology; Aritra Bhattacharjee, Khadar Mohammad, Mahesh Kulkarni, Jianmin Guo, Xing Liu and Purnima Prabhakar Kulkarni ID 10: A Fast and Efficient MPPT Converter for Solar Energy Harvesting With Cold-startup and Over-voltage Protection; Aditi Chakraborty and Ashis Maity ID 70: A PVT Adaptive Robust Data Retention Scheme for SRAM; Ashish Kumar	Student Research Forum SID-9 : Field Free Switching of 2D Material Based SOT-MTJ for LiM Applications; Shashidhara M, Shobhit Srivastava, Sourabh Panwar, Abhishek Acharya (Sardar Vallabhbhai National Institute of Technology Surat) SID-11: Enhancing Security Features of Network-on-Chip Using Lightweight Cryptosystem, Trust-Aware Routing, and Anonymous Communication; Syam Sankar, John Jose (Indian Institute of Technology Guwahati) SID-17 : Automated Synthesis and Verification of Masked Cryptographic Designs; Nilotpola Sarma, Chandan Karfa (Indian Institute of Technology Guwahati) SID-20 : Pushing the Bounds of Energy Efficient Computing Using Synthesizable Analog Cells; Ankita Nandi (Indian Institute of Science) SID-22 : Securing Nano-Circuits Against Optical Probing Attack; Sajjad Parvin (University of Bremen); Frank Sill Torres (German Aerospace Center); Rolf Drechsler (University of Bremen/DFKI) SID-33 : PVT Invariant Energy Efficient Compute-In Memory Hardware;	SRF Poster
4:35 PM	4:55 PM	0:20	PaperID: 357, Title - Constructing Rectilinear Steiner Minimum Tree with Conditional Generative Adversarial Network, Authors- Kritanta Saha, Pritha Banerjee and Susmita Sur-Kolay	PaperID: 53, Title - Efficient Mitigation of DRAM Row Buffer Conflict using Request Clustering in Manycore Systems, Authors - K Chitra, Arjun Dey and Aryabartta Sahu	PaperID: 96, Title - CMOSP18 FDSOI Technology based MCU Achieving High Performance of 1.2GHz using High Speed, Optimized Leakage & High Density Tightly Coupled Memory (TCM), Authors - Praveen Verma, Anuj Dhillon, Ashfaque Ahmed, Yagnesh Vaderiya, Chandan Singh, Veenita Kumari and Harshit Sharma	WiE-Panel: Panel discussion - Women in Semiconductor Innovation: Emerging technology trends Manisha Gambhir (Marvell) , Hemangee Kapoor (IIT- Guwahati) , Aparna Mandke (AMD), Sayalee Gharat (Siemens) . Moderator: Nithya			SRF Poster

								Sai Shubham (Indian Institute of Technology Gandhinagar) SID-34 : Optimizing RISC-V Architecture with Custom NoC for Safety and Security of the Systems; Mekala Bindu Bhargavi, Soumya J (BITS Pilani, Hyderabad Campus) SID-43 : GenAccel: A Framework to Generate Custom Heterogeneous Vector Accelerators on FPGAs; Jay Shah, Nanditha Rao (International Institute of Information Technology Bangalore) SID-46 : Flexible Electronics for Smart Sensing Systems; Suyash Shrivastava, Pydi Ganga Bahubalindruni (IISER BHOPAL) SID- 51 : Low Power Area Efficient Circuit Design for Neuromorphic Applications based on Band-to-Band Tunneling; Abhishek Kadam (Indian Institute of Technology Bombay) SID- 84 : Improving Lifetime and Performance of Non Volatile Memory Caches; Sivakumar S, John Jose (Indian Institute of Technology Guwahati)		
4:55 PM	5:15 PM	0:20	PaperID: 350, Title - Physical insights into the leakage mechanisms governing the scaling trends in 4H-SiC based junctionless FETs, Authors - jaspreet singh, Aakash Kumar Jain and M. Jagadesh Kumar	PaperID: 79, Title - FPUGen: A FrameWork to Generate Custom Floating Point FMA Accelerators on FPGAs, Authors - Himanshu Kumar Rai, Aishwarya Sridhar, Wolfgang Ecker and Nanditha Rao	PaperID: 176, Title - A Low-Power, Low-Noise, High-Performance Re-Convergent Clock Mesh Design for Large AI Compute Clusters, Authors - Hari Vinay Kancharla and Sounil Biswas	WiE-Panel(Continue)	PaperID: 368, Title - A Fully Autonomous 1.2A Auxilliary Buck DC-DC Converter for Fast Transient Load-on-Demand, Authors - Shivam agarwal, Guddanti Sivasai and Qadeer Ahmad Khan	Startup: Masterclass "The Journey of an India Semiconductor Startup" Hemant Mallapur, Tejas Networks	
5:15 PM	5:35 PM	0:20	PaperID: 64, Title - Interconnect Optimization for Timing and Power [IOTAP], Authors - Sourav Saha, Sagar Rana, Keshav Patil and Nahamaheswar Harivelam Srinivas Gari	PaperID: 241 (Test & Verification), Title - FARAD: Automated Formal Verification of Approximate Restoring Array Dividers, Authors - Chandan Kumar Jha, Khushboo Qayyum, Muhammad Hassan and Rolf Drechsler	PaperID: 107, Title - Optimizing bandwidth utilization through word based compression in Main Memories, Authors - Harsh Verma, Aswathy NS and Hemangee Kapoor	WiE-Fireside chat - Women in Research - Prof. Enakshi B. (IIT Chennai) : Moderator : Shruti. Closing remarks by Jyotika Athavale (IEEE CS & WIE)	PaperID: 311, Title - Reliable High-Performance Programmable Voltage Regulator with 0.55A Sink Current for Cryo-Cooler Electronics in 0.18µm HV-CMOS Technology, Authors - Nishant Kumar, Dr. Hari Shanker Gupta and Nihar Ranjan Mohapatra	Startup: Masterclass "India Semiconductors and Electronics Startups – an Investor View" Satish Mugulavalli, Rulezero	
5:35 PM	6:15 PM	0:40	Tea Break							
			Banquet and Awards Ceremony							
6:15 PM	6:20 PM	0:05	Opening Remarks							
6:20 PM	6:35 PM	0:15	Chief Guest Address : Mr. Priyank Kharge, Honorable Minister for IT & BT, Govt. of Karnataka							
6:35 PM	6:45 PM	0:10	CDAC: 500 RISC-V Electronic Kits - Distribution to 100 Schools by the Dignitaries							
6:45 PM	7:15 PM	0:30	Fireside Chat : "Semiconductors as a catalyst for Emerging Technologies" Sandeep Bharathi, CDO, Marvell Technology, Hitesh Garg VP & Country Head, NXP Semiconductors, Patrick Johnson, SVP, Microchip Technology							

7:15 PM	8:00 PM	0:45	Presentation of Awards : Mr. Priyank Kharge, Honorable Minister for IT & BT, Govt. of Karnataka & Dr. Ekroop Caur, Secretary for IT & BT, S & T, Govt. of Karnataka Conference Awards, VSI Women Achiever Award, VSI Lifetime Achievement Award
8:00 PM	9:30 PM	1:30	Dinner

Sheet 5: *8th Jan - C3*

Start	End	Duration	8 January, 2025 - Wednesday					
8:00 AM	9:15 AM	1:15	Registration					
9:15 AM	9:30 AM	0:15	Welcome and Recap of Day 1, Day 2					
9:30 AM	9:50 AM	0:20	Keynote: "Case for a Foundry Model for Memory Technologies - PiM as a Driver of Memory Specialization and Innovation" Prof. Mircea R. Stan, University of Virginia					
9:50 AM	10:10 AM	0:20	Keynote: "System Scale : A paradigm shift for next Gen Data Centers/AI" Wilfred Gomes, Ex Intel Fellow, Microprocessor Design and Technology					
10:10 AM	11:00 AM	0:50	Panel Discussion : "Building the Future: Semiconductor Manufacturing from Tech to Business" Ruchir Dixit - Siemens EDA, Paul Ilanghovan - Kaynes Semicon, Sana Shaikh - Synopsys, Jerry Arucan Agnes - CG Semi, Chandrashekar Chikkalingaiah - GlobalFoundries Moderator: Rajesh Nair - Tata Electronics					
11:00 AM	11:30 AM	0:30	Tea Break					
11:30 AM	11:50 AM	0:20	Keynote : “Opportunities in an AI-driven Era ” Jaswinder Ahuja, Corporate VP & MD India, Cadence					
11:50 AM	12:10 PM	0:20	Keynote: "AI In Semiconductors" Balajee Sowrirajan, MD, SSIR					
12:10 PM	1:00 PM	0:50	Panel Discussion : "Talent Generation in India: Building Semiconductor Workforce for the Future" Bhavesh Budhabhatti - IBM, Venkatesh Narasimhan - Silicon Labs, Jayraj Nair - Ansys, Gopal Koreme - Quest Global, Shivananda Koteshwar - Astera Lab Moderator: Ravi Shankar R - Proxelera					
1:00 PM	2:00 PM	1:00	Lunch Break					
			Royal Ball Room (First floor)	**Diya (First floor)**	**Turret (First floor)**	**Maharaja (Ground floor)**	**Jamavar (Ground floor)**	**Grand Ball Room (First floor)**
			Track: Hardware Security **Session chairs- Chester Rebeiro**	**Track: Logic & Circuit Design** **Session chairs- Debayan Das**	**Track: Quantum & Neuromorphic Computing** **Session chairs- Debjyoti Bhattacharjee**	**Track : 3D IC & In-Memory Computing** **Session chairs- John Jose**	**Track: Startup Forum** **Session chair - Venkatesh Narasimhan**	**Track: Industry Forum** **Session chair - Prasad Joshi**
2:00 PM	2:20 PM	0:20	PaperID: 78, Title - SHAKTI: Securing Hardware IPs by Cascade Gated Multiplexer-based Logic Obfuscation, Authors - Jugal Gandhi, Nikhil Handa, Abhay Nayak, Diksha Shekhawat, M. Santosh, Jaya Dofe and Jai Gopal Pandey	PaperID: 278, Title - Leveraging Dual Output LUTs with Pipelining for Efficient BCD to Binary Converter on FPGA, Authors - SANTOSH KUMAR and Ayan Palchaudhuri	PaperID: 114, Title - Investigating Impact of Bit-flip Errors in Control Electronics on Quantum Computation, Authors - Subrata Das, Avimita Chatterjee and Swaroop Ghosh	Invited Talk on "The story of AI Interconnects: Where Electrons Meet Photons" by Prof. Shalabh Gupta	Startup Forum Bharat Pi Aryabhata Circuits and Research Labs Vyoma Systems Private Limited Aasma Aerospace VLSIPRO TECHNOLOGIES PVT LTD Black Falcon Small Signals India Pvt Ltd	Industry Forum - Automotive Evolution : SDV Platform with High-Performance Compute Solutions , Yogesh Mittal, Renesas
2:20 PM	2:40 PM	0:20	PaperID: 381, Title - NSGA-RM: NSGA-II evolved Performance Optimized Non-Homogeneous Recursive Polynomial Multiplier Architectures, Authors - Daksh Sharma, Vasanthi D R, Sanampudi Gopala Krishna Reddy and Madhav Rao	PaperID: 228, Title - An SRAM-based Multi-Operand Architecture Implementing Multi-Bit Boolean Functions Using In-Memory Periphery Computing, Authors - Dhayan Dhananjaya Senanayake, Priyanshu Tyagi, Sparsh Mittal and Rekha Singhal	PaperID: 202, Title - An Experimental Demonstration of Neuronal Somatic Behavior Using 2D SnS Memristive Switching Characteristics and its Equivalent Circuit for Spiking Neural Network, Authors - Surya Shankar Dan	PaperID: 253, Title- Unguided Machine Learning-based Computation Offloading for Near-Memory Processing, Authors - Satanu Maity, Manojit Ghose, Avinash Kumar, Anol Chakraborty and Ankit Chakraborty		Industry Forum - Future of Semiconductor Industry - One Chip vs Many Chiplets, Manoj Dusanapudi, IBM

2:40 PM	3:00 PM	0:20	PaperID: 145, Title - CRIS-b: A High-Speed Unified Modulo Reduction Algorithm and Hardware Architecture for CRYSTALS-Kyber, Authors - Rahul Shrestha and Alip Majumdar	PaperID: 143, Title - Serialized Control Interface ASIC for Distributed Controllers of Space-borne RADAR, Authors - Chiragkumar B. Patel, Ajay Kumar Singh, Himanshu N. Patel and B Saravana Kumar	PaperID: 325, Title - ATRIAL FLUTTER DETECTION SYSTEM BY AdEx ENCODED LEAD-II ECG, Authors - Sushmi R, Priya K and Binsu Kailath	PaperID: 117, Title - A Study on the Impact of Temperature-Dependent Ferroelectric Switching Behavior in 3D Memory Architecture, Authors - Varun Darshana Parekh, Yi Xiao, Yixin Xu, Zijian Zhao, Zhouhang Jiang, Rudra Biswas, Sumitha George, Kai Ni and Vijaykrishnan Narayanan		Industry Forum - Edge Computing - Redefining Intelligent Systems in AI and Digital Era, Vishal Patil, Moschip
3:00 PM	3:20 PM	0:20	PaperID: 116, Title - Novel Hardware Architectures for PRESENT Block Cipher and its FPGA Realizations, Authors - RUBY MISHRA, Manish Okade and Kamalakanta Mahapatra	PaperID: 256, Title - Fast Bit-Sliced VLSI Architectures on FPGA for Montgomery Domain Modular Inversion, Authors - SOHAM ADHIKARY and Ayan Palchaudhuri	PaperID: 302, Title - Quantum Analysis of LESCA, Authors - Sumanta Chakraborty, Debajyoti Mandal and SK Hafizul Islam	PaperID: 329, Title - DNA-CIM: DNA Sequence Analysis using RRAM-based Compute In-Memory Accelerator, Authors - Chithambara Moorthii J, Anmol Singla and Manan Suri		Industry Forum - Wireless in the Chiplet Age, Purbasha Rakshit, Sasken
3:20 PM	3:50 PM	0:30	Tea Break					
			Royal Ball Room (First floor)	**Diya (First floor)**	**Turret (First floor)**	**Maharaja (Ground floor)**	**Jamavar (Ground floor)**	**Grand Ball Room (First floor)**
			Track: Analog and Mixed Signal Design **Session chairs- Subrahmanyam Boyapati**	**Track: Emerging Technologies & Circuit Design** **Session chairs- Debayan Das**	**Track - EDA & CAD** **Session chairs- Anand Bulusu**	**Track: AIML Hardware Accelerators** **Session chairs- Viveka K R**	**Track : Design Contest** **Session chair - Nanditha Rao**	**Track: Industry Forum, Startup Forum** **Session Chairs : Prasad Joshi, Venkatesh Narasimhan**
3:50 PM	4:10 PM	0:20	Invited Talk on "Essential connectivity in the world of AI: Analog and beyond" by Manisha Gambhir	PaperID: 201, Title - Tunnel Magnetoresistance in Strained L10-FeAu Perpendicular Magnetic Tunnel Junction, Authors - Rouf Rahman Sheikh and Ram Krishna Ghosh	PaperID: 149, Title - PPA-aware Power Grid Optimization Techniques for Congested High Frequency Datapath Designs, Authors - Cheryl Mary Joyce, Parag Upadhyay, Sashank Nishad and Abhimanyu Kakkar	PaperID: 83, Title - A 0.75mm2 407µW real-time speech audio denoiser with quantized cascaded redundant convolutional encoder-decoder for wearable IoT devices, Authors - Dimple Vijay Kochar, Maitreyi Ashok and Anantha P. Chandrakasan	Microchip : Hardware Software Co-Design of Multi Receiver Narrowband Spectrum Sensing for Cognitive Radio using Deep Learning : Sardar Vallabhbhai National Institute of Technology Securing and Accelerating Vehicle-to-Vehicle Communications to combat Cyber-Threats and enabling ML-Based intelligent decision in Autonomous Vehicles : Indian Institute of Technology - Patna A Dual-Mode Assistive and Therapeutic Device for Enhanced Hand Mobility Using Myoware Sensors and Soft Robotics : International Institute of Information Technology - Bangalore Project Insight : Kumaraguru College of Technology AI Driven Retail Automation : IIIT - Kottayam NXP: Hey Auxi!!: Your All-in-One Interactive Home Companion : Amrita School of Engineering MoodSync: Emotion-Based Music/Visual Effects Recommendation through Wearables : International Institute of Information Technology Museum Guide Robot with RFID-Based Artifact Detection and Sign Language Support : Rajiv Gandhi University of Knowledge Tec	Industry Forum - How the Service Eco system can augment edge computing solutions, Sudipto Das, Quest Global
4:10 PM	4:30 PM	0:20	PaperID: 104, Title - 8GHz Multi-Phase Ring VCO Design with Wide Tuning Range for SerDes Applications in 6nm FinFET Process, Authors - Ravuru Vasudeva Reddy, Siva Kumar Rapina, Siddhartha Hazra and Dr K Sarangam	PaperID: 272, Title - Optimization of Sub-threshold Standard Cells for Energy Efficient Designs, Authors - Vardhan Suroshi, Karthik B K, Vikram Kannur, Vinay Reddy and Madhura Purnaprajna	PaperID: 354, Title - Symmetry-Based Synthesis For Interpretable Boolean Evaluation, Authors - Andrea Costamagna, Alan Mishchenko, Satrajit Chatterjee and Giovanni De Micheli	PaperID: 98, Title - E-DOSA: Efficient Dataflow for Optimising SNN Acceleration, Authors - Binayak Behera, Imlijungla Longchar and Hemangee Kapoor		Industry Forum - AI Driven Custom Silicon, Amudhan Balasubramanmanian, HCL
4:30 PM	4:50 PM	0:20	PaperID: 218, Title - Precision Clock Generation with Reference clock Loss Tolerant Dynamic Tuning to enable Crystal less SSD, Authors - Pikul Sarkar, Nitin Gupta, Pallat Aravind, Bhavin Odedara and Dror Shahar	PaperID: 369, Title - HyCMAx: Power-Efficient Hybrid CMOS-Memristor-Based Approximate Dividers for Error-Resilient Applications, Authors - Monika Pokharia, Het Trivedi, Siddharth Doshi, Ravi Hegde and Joycee Mekie	PaperID: 84, Title - DuRTL - Information Flow Analysis Tool for Register Transfer Level Hardware Designs, Authors - Lutz Schammer, Gianluca Martino and Goerschwin Fey	PaperID: 47, Title - A Study on Efficiency Improvements of DNN Accelerators via Denormalized Arithmetic Elimination, Authors - Alexander Kharitonov and Sandip Kundu		Startup Forum Green PMU Semi Private Limited InCore Semiconductors Trans Vitals Pvt. Ltd

							e-SAM (Electronic Secure Asset Management) : RV College of Engineering YOG GURU - AI-Integrated Smart Yoga Device for Personalized Yoga Experience : Thapar University Texas Instruments : Body Vitals Extraction : IIT - Indore Warehouse Management System using Autonomous Robots and Centralized Coordinator : International Institute of Information Technology, Bangalore Hardware Implementation of Video Violence Recognition and Women Tracking based Surveillance System using Machine Learning : M S Ramaiah University of Applied Science Real Time LLVE : National Institute of Technology Karnataka, Surathkal Helmet detection : National Institute of Technology, Manipur	
4:50 PM	5:10 PM	0:20	PaperID: 252, Title - A Wide Dynamic Range Differential Drive CMOS Rectifier for µWatts RF Energy Harvesting Systems, Authors - Chaya Hegde, Arun Mohan, Saroj Mondal and Roy P. Paily	PaperID: 375, Title - K Band High Power Broadband AlGaN/GaN HEMT Balanced Power Amplifier for Satellite Transponder, Authors - Ritan Das and Basudev Majumder	PaperID: 137, Title - 2D Thermal Contour Modeling of 14 nm SOI FinFET using Machine Learning for Efficient, Authors - Banit Negi, Hariharan Muthusamy and Vivek Kumar	PaperID: 251, Title - BMC Engine Sequencing with Graph Neural Network Embeddings of Hardware Circuits, Authors - Soumik Guha Roy, Adriz Chanda, Prateek Ganguli, Sumana Ghosh, Ansuman Banerjee, Raj Kumar Gajavelly and Surendran Sudhakar		
5:10 PM	5:30 PM	0:20	PaperID: 95, Authors - Startup Circuit For Relaxation Oscillators With Low Functional Current And Minimal Area, Authors - Anubhav Srivastava, Sadique Mohammad Iqbal, Divya Tripathi and Saurabh Goyal	PaperID: 3, Title - TOGGLE6.0 -- A 4.8Gbps Next Generation Area and Power Efficient Transceiver for Flash Memory Interface, Authors - Hari Vijay Venkatanarayanan, Rustum Prasad Sahu, Maheswara Alamuru, Ergam Reddy Battini, Syed Mohammed Haroon, Saurav Suman, Deepika Mallela, Sanjeeb Kumar Ghosh and Billy Koo"	PaperID: 316, Title - Codesign for Broadcast Addressing Biochip towards Tamper-Resistance and Enhanced Reliability, Authors - Ritwika Majumdar, Piyali Datta, Arpan Chakraborty and Rajat Kumar Pal	PaperID: 303, Title - Accelerated Design Verification Coverage Closure using Machine Learning, Authors - Shivani Jayakumar, Prasanth Viswanathan Pillai and Sumit K. Mandal		