Start Time	End Time	DAY-1 | 10-Jan-2023 | Tuesday
PLENARY - HALL 3		
0800 hrs	Onwards	Spot Registrations
0930 hrs	1030 hrs	Inauguration Ceremony (Shri Rajeev Chandrasekhar, Shri K T Rama Rao, Shri Jayesh Ranjan, Shri. Victor Peng, Shri. Shashi Reddy, Smt. Jaya Jagadish, Shri. Venkata Simhadri, Shri. Satya Gupta)
1030 hrs	**1100 hrs**	**EXHIBIT AREA INUGURATION & TEA BREAK**
1100 hrs	1130 hrs	Keynote Address | Victor Peng, President, AMD | High performance, adaptive, heterogeneous computing for the intelligent digital world
1130 hrs	1155 hrs	Keynote Address | Assaf Touboul, VP, Qualcomm | 5G Opportunities, Challenges, and Path to 6G
1155 hrs	1220 hrs	Keynote Address | Dr. Prith Banerjee, CTO, Ansys | Future of Simulation Driven Innovation for Nanotechnology Research
1220 hrs	1245 hrs	Keynote Address | Prof. Kaushik Roy, Purdue University | Rethinking Computing with Neuro-inspired Learning: Algorithms, Circuits, and Devices
1245 hrs	1255 hrs	Keynote Address | Dr. Venkat Mattela, Founder & CEO, Ceremorphic Inc., |Challenges and opportunities for semiconductors in Artificial Intelligence (AI) era.
1255 hrs	**1400 hrs**	**LUNCH BREAK**

Venue		HALL-3	HALL-5	MRG 1,2	HALL-6
Tracks Open		**Track 1A- Technical Track Embedded Systems Design**	**Track 1B- Technical Track Analog & Mixed Signals**	**Track 1C- User Design Track**	**Track 1D- Industry Forum-Keynotes 5G Opportunities & Challenges**
1400 hrs	1420 hrs	Invited Talk | Research Opportunities in Cyber Physical System Design | Bishnu Prasad Das, IIT Roorkee	Invited Talk | Multi-Channel Analog-Digital Conversion using Delta-Sigma-Modulators Without Reset | R S Ashwin Kumar, IIT Kanpur	A Novel Adiabatic PUF for Portable Devices | Vishnu Bajjuri, Nalesh S and Kala S	Keynote Address | Mohan Rao, Corp VP & CTO, Samsung Research India
1420 hrs	1440 hrs	Hardware Architecture and FPGA Implementation of Low Latency Turbo Encoder for Deep-Space Communication Systems | Meghvern Pathak, Rahul Shrestha (IIT Mandi)	A Low Noise Bandgap Reference with 0.89 V Vref , 0.88 µV rms noise and 80 dB of PSRR | Sowmyashree, Hitesh Shrimali (IIT Mandi)	Physical Implementation of Functional Safety (FuSa) Features in Automotive Chips | Shashikiran Srinivasa and Badri Ramasubramanian	
1440 hrs	1500 hrs	Lightweight Approximate Multiplier with Improved Accuracy in FPGA for Error Resilient Application | Apurba Prasad Padhy, Bishnu Prasad Das (IIT Roorkee)	Radiation Hardened CMOS Programmable Bias Generator for Space Applications at 180nm | Ashutosh Yadav, Anand Bulusu (IIT Roorkee) ; Surinder Singh (SCL); Sudeb Dasgupta (IIT Roorkee)	Design and Optimization of FinFETs using Machine Learning Methods | Hemalatha murugan, P Aravind Raj, N B Balamurugan, M Suguna and V Kavithanjali	Keynote Address | Muralikrishnan B, President, Xiaomi India
1500 hrs	1520 hrs	Delay-Aware Control for Autonomous Systems | Sumana Ghosh (ISI Kolkatta)	A low-power resistive tail dynamic comparator with self-shut mechanism | Sanjoy Kumar Dey (Intel); Mukul Sarkar, Shouribrata Chatterjee (IIT Delhi)	A frequency optimized linear scalable architecture for CNN Interface on FPGAs | Shubhayu Das, Nanditha Rao and Sharad Sinha	Keynote Address | Arif Adoni, Head-Product Engineering | Bharti Airtel

1520 hrs	1540 hrs	Hardware implementation of Ring-LWE lattice cryptography with BCH and Gray coding based error correction | Somnath Mondal, Sachin Patkar (IIT Bombay); T K. Pal (DRDO)	A Sense Amplifier Based Bulk Built-In Current Sensor for Detecting Laser-Induced Currents | Debjit Batabyal, Sandeep Kumar Singh, Rajnish Kumar Mishra, Anuj Grover (IIIT-Delhi)	Energy Efficient Approximate Floating Point Divider | Noor Mahammad Sk, Sreehari Veeramachaneni, Ayesha Sk and Namratha Nadh Jammalamadugu	
1540 hrs	**1600 hrs**	**TEA BREAK**			
Tracks Open		**Track 2A- Technical Track Low Power Digital Architectures**	**Track 2B- Technical Track Advances in CAD & VLSI**	**Track 2C- User Design Track**	**Track 2D-Industry Forum-Panel Discussion 5G Usecases & how to transform businesses and industries**
1600 hrs	1620 hrs	Invited Talk: Compute Efficient and Configurable Architecture of Deep Neural Network Accelerator | by Santosh Kumar Vishvakarma, IIT Indore	Invited Talk: Variability Aware Timing Analysis considering Device/Layout level phenomena at circuit level abstraction | Anand Bulusu, IIT Roorke	Retention leakage reduction in SRAM using Adaptive Bias Control | Ashish Kumar, STMicroelectronics	Moderator | Sanjay Razdan, Sr. Director, Qualcomm India Member | Assaf Touboul, VP Technology, Qualcomm Israel Member | Tasleem Arif, Managing Director, Oppo & Oneplus R&D Member | Charles Santhosam, Asso. VP, Mavenir India Member | Girish Baliga, Gen. Mgr - Industry Mktg, Keysight Technologies. Member | Satish Jamadagni, Sr. VP, Reliance Jio
1620 hrs	1640 hrs	Design of Hardware Efficient Approximate DCT Architecture | Vishwajeet S B, Vaibhavi Solanki, A. D. Darji (Sardar Vallabhai NIT)	Translation of Array Expressions for In-Memory Computation on Memristive Crossbar | Sumanta Pyne (NIT, Rourkela)	Activity based frequency scalar for Network-On-Chip Idle Power Reduction | Krishnan Ananthanarayanan and Santosh Kumar Singh	
1640 hrs	1700 hrs	Design of Energy Efficient and Low Delay Posit Multiplier | Lakshmi Bhanuprakash Reddy Konduru, R S Haripriya, Keerthija Puli (IIT Tirupati) ; Subba Ramkumar Reddy Annapalli (Intel); Vikramkumar Pudi (IIT Tirupati)	ASPIRE: An Intermediate Representation for Abstract Security Policies | Padmaja Bhamidipati, Ranga Vemuri (University of Cincinnati)	Optimal Clock tree synthesis for high frequency SoCs | Naga Teja Babu, Subba Ramkumar Reddy Annapalli and Pallapu Lakshmi Sarvaani	

1700 hrs	1720 hrs	Surmounting Challenges in the Design of Low Power Real Time Clock IP For Advanced FinFET Technology Nodes | Krishnan Sukumar, Santosh Vodnala, Ravindra Ayyagari, Animesh Jain, Thanapandi Ganesan, Rajesh R (AMD)	MLTDRC: Machine Learning Driven Faster Timing Design Rule Check Convergence | Santanu Kundu, Chetan Suryakant Padharia, Ravi Sankar Kerla (Intel)	Implementation of multiple DFT techniques for power efficient testing | Moksh Sancheti	
1720 hrs	1740 hrs	Dynamic Keeper for 1R1W 8T-SRAM to enable Read Operation at 150c till 0.5v in 5nm FinFET | Vinay Kumar, Vijay Sahu, Ambar Kanda, Sudhir Kumar (Synopsys)	A Machine Learning-based model for Single Event Upset Current Prediction in 14nm FinFETs | Vibhu V, Sparsh Mittal, Vivek Kumar (IIT Roorkee)	Advanced ATPG Fault Models | Kishan Mayani, Krushnakant Kori and Saumya Shah	
Poster Session | Hall-4 10-Jan-1700-1830 hrs	Post Silicon Validation for I2C (SMBUS) Peripheral | Swati Shilaskar, Ketki Sonawane (VIT Pune) ; Anup Behre (Seagate); Shripad Bhatlawande (VIT Pune) ;				
	Efficient FPGA Implementations of Lifting based DWT using Partial Reconfiguration | Mohamed Asan Basiri, PVSR Bharadwaja (IITDM Kurnool)				
	Accelerating Defect Simulation in Analog and Mixed-Signal Circuits by Parallel Defect Injection | Sayandeep Sanyal (IIT-Kharagpur); Mayukh Bhattacharya (Synopsys); Pallab Dasgupta, Amit Patra (IIT-Kharagpur) ;				
	Mutual Information based Efficient Spike Encoding on FPGA | Omkareshwar Gundoji, Dighanchal Banerjee, Sounak Dey, Arpan Pal (TCS Research)				
	SANNA: Secure Acceleration of Neural Network Applications | Akash Poptani, Abhishek Mittal, Rishit Saiya, Rajshekar Kalayappan (IIT Dharwad); Sandeep Chandran (IIT Palakkad)				
	The Acceleration of OPUS Codec Using Processor – FPGA Co-processing | Sunny Bezawada, Prakash Reddy Battu (Microchip)				
	A 105-525MHz Integer-N Phase-Locked Loop in Indigenous SCL 180nm CMOS | Shivam Nigam (IIT Madras); Mukund Murali (Qualcomm); Saurabh Saxena (IIT Madras); Hari Shanker Gupta (SAC-ISRO)				

		Evaluating the Impact of Transition Delay Faults in GPUs | Josie E. Rodriguez Condia, Matteo Sonza Reorda (Politecnico di Torino)
		An Energy-Efficient Multi-bit Current-based Analog Compute In-Memory Architecture and Design Methodology | Dinesh Kushwaha (IIT Roorkee); Ashish Joshi (Intel); Neha Gupta, Aditya Sharma (IIT Roorkee); Sandeep Miryala (Brookhaven National Lab, NY); Rajiv V. Joshi (T.J. Watson, NY); Sudeb Dasgupta, Anand Bulusu (IIT Roorkee);
		Reliability Enhancement of Hardware Trojan Detection using Histogram Augmentation Technique | Vaishnavi Sankar, Balachander S, Nirmala Devi. M, Jayakumar M (Amrita Vishwa Vidyapeetham)
		DARK-Adders: Digital Hardware Trojan Attack on Block-based Approximate Adders | Vishesh Mishra, Neelofar Hassan, Akshay Mehta, Urbi Chatterjee (IIT Kanpur)
		True Random Number Generator based on modified Voltage-Gated Spintronic structure | Alisha P B, Tripti S Warrier (Cochin University of Science and Technology)
		A Novel Approach for Assisting Blind People Using a Smart Wearable Device | Shyam Peraka, SK Irfan Ali, Reddy Sudheer, Pilli Praveen Kumar, Goutham Kondala, Dimple Samal (RGUKT-Nuzvid)
		Word-Level Structure Identification In FPGA Designs Using Cell Proximity Information | Aparajithan Nathamuni-Venkatesan, Ram-Venkat Narayanan, Kishore Pula, Sundarakumar Muthukumaran, Ranga Vemuri (University of Cincinnati)
		Analysis and Design of Low Phase Noise 20 GHz VCO for Frequency Modulated Continuous Wave Chirp Synthesizers in mmWave Radars | Harikrishna Kambham, Srayan Sankar Chatterjee, Adithya Sunil Edakkadan, Abhishek Srivastava (IIIT-Hyderabad)
		InsectEye: An Intelligent Trap for Insect Biodiversity Monitoring | Eric Homan, Codey Mathis, Chonghan Lee, Harland Patch, Christian Grozinger, Vijay Narayanan (The Pennsylvania State University)
		An mmWave Frequency Range Multi-Modulus Programmable Divider for FMCW Radar Applications | Sresthavadhani Mantha, Adithya Sunil Edakkadan, Arpit Sahni, Abhishek Srivastava (IIIT Hyderabad)
Start Time	**End Time**	**DAY-2 | 11-Jan-2023 | Wednesday**

MORNING SESSION: 0930 hrs - 1300 hrs		
0900 hrs	0925 hrs	Keynote Address | Ruchir Dixit, VP & Country Manager-Siemens EDA | System Design 'X' factor for the Semiconductor Industry
0925 hrs	0950 hrs	Keynote Address | Bruce Weyer, Corp. VP, FPGA BU, Microchip | Empowering People to Excite Innovation
0950 hrs	1010 hrs	Keynote Address | Prof. Shanthi Pavan, IIT Madras | Continuous-Time Pipelined Converters - Where Filtering Meets Analog-to-Digital Conversion
1010 hrs	1035 hrs	Keynote Address | Noam Mizrahi, CTO & Sr. Fellow, Marvell | An Infrastructure for Scale
1035 hrs	1055 hrs	Keynote Address | Manish Kothari, SVP Silicon Labs | The Growth of the IoT – It starts with Silicon
1100 hrs	1130 hrs	**TEA BREAK / POSTER SESSION**
Industry Forum- Semiconductor Manufacturing in India		
1130 hrs	1150 hrs	Keynote Address | Tushar Dhayagude, VP,Transphorm Inc
1150 hrs	1205 hrs	Keynote Address | Anant Naik, CEO, Gaetec
1205 hrs	1300 hrs	Panel Discussion | Semiconductor Manufacturing in India Moderator | Venkata Simhadri, MD & CEO, MosChip Member | Suraj Rengarajan, CTO, Applied Materials Member | Harpreet Singh Jatana, SCL- ISRO Member | Anand Muthaiah, VP,Tessolve

		Member | Devesh Dwivedi, India Site Head, GlobalFoundries Member | Brahmanand Reddy Patil, Managing Director, Vector Informatik			
1300 hrs	**1400 hrs**	**LUNCH BREAK / POSTER SESSION**			
Tracks Open		**Track 3A- Technical Track Test & Reliability**	**Track 3B- Technical Track Analog & Mixed Signals-2**	**Track 3C- Technical Track HW for AI/ML**	**Track 3D- Industry Forum-Keynotes Automotive Innovations for Sustainable & Safe Mobility**
1400 hrs	1420 hrs	Invited Talk | Logical Locking, hardware security | Ujjwal Guin, Auburn University	Invited Talk | Active Clamp Flyback controllers paired with GaN FETs in High Density AC/DC Power Supplies | Ahsan Zaman, Silanna Semiconductor	Invited Talk | Next generation AI hardware | Alex James, Digital University Kerala	1400-1430 hrs | Keynote Address | Ravi Koodli Nagaraj, Sr. Director, Automotive Design Center, STMicroelectronics 1430-1500 hrs | Keynote Address | Venkat Rajaraman, Founder & CEO, Cygni Energy Pvt Ltd 1500-1530 hrs | Keynote Address | Amardeep Punhani, Sr. Director-R&D, Digital Design, NXP Semiconductors
1420 hrs	1440 hrs	Efficient MBIST Area and Test Time Estimator Using Machine Learning Technique | Darakshan Jamal, Ratheesh Veetil (Intel)	Unifying Intrinsically-Operated Physically Unclonable Function and Random Number Generation in Analog Circuits: A Case Study on Successive Approximation ADC | Ahish Shylendra (UIUC) ; Swarup Bhunia (Univ of Florida); Amit Ranjan Trivedi (UIUC)	Extending Action Recognition in the Compressed Domain | Samuel Abrams, Vijaykrishnan Narayanan (The Pennslyvania State University)	
1440 hrs	1500 hrs	A Novel AI Based Approach for Performance validation | Kahkeshan Naz, Rohit Jindal, Sai Boothkuri (Intel)	Programmable Delay Line With Inherent Duty Cycle Correction | Siva Charan Nimmagadda, Hari Bilash Dubey (AMD)	Design and Analysis of POSIT Quire Processing Engine for Neural Network Applications | Pranose J Edavoor, Aneesh Raveendran, David Selvakumar, Vivian Desalphine, Dharani Shankar G, Gopal Raut (CDAC)	

1500 hrs	1520 hrs	Signal Agnostic Scalable SCAN Wrapper Design | Hanumantharaya H, Ratheesh T Veetil, Anvesh Gadi (Intel)	A 2.25 GHz PLL with 0.05-2 MHz Inloop Phase Modulation and -70 dBc Reference Spur for Telemetry Applications | Snigdha Jakkoju, Deepthi J. Bandarupalli (IIT Madras); Anil Srikanth (Texas Instruments); Saji Thomas (Vikram Sarabhai Space Center); Saurabh Saxena (IIT Madras)	Fast and Robust Sense Amplifier for Digital In Memory Computing | Kailash Prasad, Ayush Srivastava (IIT Gandhinagar); Nistha Baruah (NIT Silchar), Joycee Mekie (IIT Gandhinagar)	
1520 hrs	1540 hrs	Mutation Analysis and Model Checking Guided Test Generation for SoC Run-Time Monitors | Suriya Srinivasan, Ranga Vemuri (Univ of Cincinnati)	Ultra-Low Power Non-Uniform SAR ADC based ECG detector for Early Detection of Cardiovascular Diseases | Aditya Ramkumar, Anshul Verma, Bishnu Prasad Das (IIT Roorkee)	MOSCON: Modified Outer Product based Sparse Matrix-Matrix Multiplication Accelerator with Configurable Tiles | Noble G (IIIT-Kottayam), Nalesh S (CUSAT), Kala S (IIIT-Kottayam)	
1540 hrs	**1600 hrs**	**TEA BREAK**			
Tracks Open		**Track 4A- Technical Track Sensors & Wireline Communication**	**Track 4B- Technical Track Latest Trends in Device Modelling**		**Track 4D-Industry Forum-Panel Discussion India on the E-mobility Highway**
1600 hrs	1620 hrs	Invited Talk | mmWave Sensing and Low Phase Noise VCOs | Abhishek Srivastava	Invited Talk | Energy-efficient 2.5D Architecture for Machine Learning Applications | Sumit Kumar Mandal		Moderator | Preet Yadav, R&D SOC Technical Program Mgr, NXP Semiconductors Member | Sanjay Gupta, President & CEO, Minda Corporation Member | Swapnil Jain, CTO, Ather Energy Member | Nithin Gupta, Sr. Director, Western Digital
1620 hrs	1640 hrs	A Portable Ultra-low-cost Multi-Gas Sensing System-on-Module for Wireless Air Quality Monitoring Network | Anamika Sharma, Sachin Divekar, Rajesh Zele (IIT Bombay)	Enhanced Performance Parameters of Magnetic Tunnel Junction with Composite Dielectric Barrier | Reshma Sinha (Shaheed Rajguru College of Applied Sciences for Women, University of Delhi); Jasdeep Kaur		

			(Indira Gandhi Delhi Technical University for Women)		
1640 hrs	1700 hrs	FPGA based Smart and Sustainable Agriculture Shyam Peraka, SK Irfan Ali, Durga Vasu Mogili, Ashok Kumar Palivela, Sudheer Reddy, Jyotsna Bavisetti, Dhanush Reddy Y (RGUKT-Nuzvid)	FEM modeling of gate resistance for 5 nm SGC/DGC Stacked Nanosheet Transistor | Vivek Kumar (NIT Uttarakhand); Jyoti Patel, Arnab Datta, Sudeb Dasgupta (IIT Roorkee)		
1700 hrs	1720 hrs	SV Based Fast & Accurate Verification Methodology for CTLE Adaptation Algorithm | Abhishek Jadhav, Varsha Bhide, T.N.V Raghuram, Tapas Nandy (Intel)	Automatic Implementation and Evaluation of Error-Correcting Codes for Quantum Computing: An Open-Source Framework for Quantum Error Correction | Thomas Grurl (Univ of Applied Sciences Upper Austria); Christoph Pichler (Johannes Kepler Univ Linz, Austria); Jürgen Fuß (Univ of Applied Sciences Upper Austria); Robert Wille (Technical Univ of Munich)		
1720 hrs	1740 hrs	A 16Gbps 3rd Order CTLE Design for Serial Links with High Channel Loss in 16nm FinFET | Pranay Thota, Siva Kumar Rapina (Microchip); Bheema Rao Nistala (NIT Warangal)	Implementation of Probabilistic Bits (Pbits) using Low Barrier Magnets: Investigation and Analysis | Amina Haroon, Ram Krishna Ghosh, Sneh Saurabh (IIIT Delhi)		
Design Contest |	**Theme | Hardware and Embedded Software co-design with hardware acceleration in SoC FPGA**				
	HW Platform | Microchip Technology's RISC-V based PolarFire SoC Icicle Kit				

Hall-4 11-Jan-2023	**Team Size | 13 Teams**
	Team-1 | Vinay Rayapati, Gogireddy Ravi Kiran Reddy, Sanampudi Gopala Krishna Reddy, Gandi Ajay Kumar, Nanditha Rao | International Institute of Information Technology, Bangalore
	Team-2 | Renjith G, Mayank Verma, Dr. Raghu CV | National Institute of Technology, Calicut
	Team-3 | M Sudarshan Shenoy, Ramesh Kini M | National Institute of Technology, Karnataka
	Team-4 | Anmol J. Shetty, Maurya Patel, Anshul Madurwar, Paras S Vekariya | IIT Bombay
	Team-5 | Syed Asrar Ul Haq, Animesh Sharma, Anurag Gulati | Indraprastha Institute of Information Technology, Delhi
	Team-6 | Bikram Paul, , Meenali Janveja, Lakshita, Korada Pavan Kumar | IIT Guwahati
	Team-7 | Neelam, Ishaan Sharma | Indraprastha Institute of Information, Delhi
	Team-8 | Anito Anto | IIT Palakkad
	Team-9 | Narayana Sri Vignesh Agarwal, Gude Sai Durga Prasad, Nakkala Sambasiva Rao, Dr.G.L.Madhumati | VR Siddharth Engineering College
	Team-10 | Sanath N U, Shashank Bhat, S K Dheraj, Nagarjun Kulkarni | BMS College of Engineering, Bangalore
	Team-11 | Sanket Patadiya, Sohankumar Patel, Umair Uzair Jarullah, Vivek Chauhan, Bhavay Savaliya, Krishil Gandhi, Mohit Sapkal | Sardar Vallabhai National Institute of Technology
	Team-12 | Ruchit Chudasama, Daniel Giftson, Tom Glint, Aryan Gupta, Joycee Mekie, Sukanya More, Vrajesh Patel, Ashiwini Pathak, Kailash Prasad, Prateek Sharma, Megha Yadav | IIT Gandhinagar

1830 hrs	2030 hrs	AWARDS EVENING FOLLOWED BY BANQUET DINNER			
1830 hrs	1845 hrs	Award Ceremony			
1845 hrs	1905 hrs	Keynote Address | Prof. Thomas Lee, Stanford University | Compute-Energy Constraints and How They'll Stimulate a New Wave of Innovation			
1927 hrs	1932 hrs	Keynote Address | Shri M M Pallam Raju, Ex.Union Minister-HRD, Founding Partner for ASIP Technologies			
1954 hrs	2004 hrs	Keynote Address | Shri Jayesh Ranjan, Principal Secretary, Information Technology (IT), Industry and Commerce; Government of Telangana			
2030 hrs	onwards	Dinner			
Start Time	**End Time**	**DAY-3 | 12-Jan-2023 | Thursday**			
MORNING SESSION: 0930 hrs - 1300 hrs					
0900 hrs	0920 hrs	Keynote Address | Sudhir Mallya, VP, Product Mktg, Alphawave | Accelerating data for a connected world: the power of optimized silicon			
0920 hrs	0940 hrs	Keynote Address | Rahul Razdan, CEO, Razdan Research Institute | AI's disruptive impact on Systems, Semiconductors, and Design			
0940 hrs	1010 hrs	Keynote Address | Vinayak Godse, CEO, Data Security Council of India | Security Agenda in Semiconductor led Disruptive Innovations			

1010 hrs	1040 hrs	Keynote Address | Prof. Makoto Ikeda, University of Tokya | Hardware acceleration of functional encryption			
1040 hrs	1100 hrs	Keynote Address | Dr. Madhav Pulipati, CEO, Photonics Corp | Alternative computing paradigms - A way forward			
1100 hrs	**1130 hrs**	**TEA BREAK / POSTER SESSION**			
1130 hrs	1150 hrs	Keynote Address | Dr. Neetha Maria Celin, Scientist E, C-DAC, Trivendrum | DIR-V VEGA Microprocessors : One step towards AatmaNirbhar Bharat			
1150 hrs	1210 hrs	Keynote Address | Naga Bharath Daka, Co-Founder, Skyroot Aerospace | Embedded systems in mission critical applications			
1210 hrs	1300 hrs	Panel Title : Evolution of Indian EDA Marketplace Moderator | Sumit Goswami, Sr. Director, Qualcomm Member | Dr. Shivananda Koteshwar, Grp. Director, Synopsys Member | Sridhar Rangarajan, Grp. Director, Cadence Member | Dipanjan Gope, CEO, Simyog Technologies Member | Ruchir Dixit, VP & Country Manager, Siemens EDA Member | Vinayakam Subramanian, Director, Ansys			
1300 hrs	**1400 hrs**	**LUNCH BREAK**			
Tracks Open		**Track 5A- Technical Track Embedded Systems Design**	**Track 5B- Technical Track Analog & Mixed Signals-3**	**Track 5C- Student Research Forum**	**Track 5D-Start-up Forum**
1400 hrs	1420 hrs	DRRA-based Reconfigurable Architecture for Mixed-Radix FFT | Reeshita Kallapu (IIT Bhubneshwar); Dimitrios Stathis (KTH Royal Inst. Of Technology, Sweden); Srinivas Boppu (IIT Bhubneshwar);	Invited Talk | Circuit-Model Co-design for Scalable, Uncertainty-Aware Compute-in-Memory Inference | Amit Ranjan Trivedi	Boolean Expression Based (BEB), DC-Balanced, Partitioned-Block,8B/10B Line Encoder | Ritu Verma, Andriy Ostapovets and Anna Serra | Institute of Physics of Materials, Czech	1405-1420 hrs : Keynote Address | Shashi Reddy, Qualcomm 1420-1435 hrs : Keynote Address | Srini Chandupatla, Manjeera Digital Systems

		Ahmed Hemani (KTH Royal Inst. Of Technology, Sweden)		Academy of Sciences, Czech Republic	1435-1450 hrs : Keynote Address | Ajay Jain, Silvermeedle Ventures 1450-1505 hrs : Keynote Address | Venkatesh Narasimhan, Silicon Labs 1505-1510 hrs : Introduction to Pitches | Sudeep, Ramesh 1510-1540 hrs : Startup Pitches | Sumedha IT | Anew Design Automation LightSpeed Photonics | VASBEAM | Cyrrup Solutions | Rapture Innovation Labs | Anscer Robotics | Hivericks Technologies | Vanix Technologies Spearix Technologies | Silizium Circuits | Krisemi Design Technologies
1420 hrs	1440 hrs	Live & Seamless Firmware Upgrade in Real Time Control Systems | Sira Rao, Baskaran Chidambaram, Prasanth V., Karthik Rajakumar, Pramod Prabhakara, Praveen Ravichandran, Shailesh Ghotgalkar, Ashish Vanjari, Mihir Mody (Texas Instruments)	Design Challenges and Techniques for 5nm FinFET CMOS Analog/Mixed-Signal Circuits | Saurabh Goyal, Sanjay Kumar Wadhwa, Divya Tripathi, Gaurav Agrawal, Krishna Thakur, Deependra Kumar Jain, Alvin L.S. Loke, Atul Kumar, Manish Kumar Upadhyay (NXP); Bhawna (Western Digital); Sanjoy Kumar Dey (Intel)	Improving Endurance of Non-Volatile Memories using Compression, Encoding and Selective Victim Caching | Arijit Nath and Hemangee Kapoor | IIT,Guwahati	
1440 hrs	1500 hrs	WIB-SAR: Write Intensity Based Selective Address Remapping | Aswathy N S, Deep Bhuinya, Hemangee K. Kapoor (IIT Guwahati)	Design of Radiation Hardened 12T SRAM with Enhanced Reliability and Read/Write Latency for Space Application | Sakib Ansari, Kavitha S (IIIT-DM Kancheepuram); Santosh Vishvakarma (IIT Indore); Bhupendra Singh Reniwal (IIT Jodhpur)	Towards Design and Implementation of a CNFET-based Ternary Logic Processor | Sharvani Gadgil and Chetan Vudadha | BITS-Pilani, Hyd	
1500 hrs	1520 hrs	Design of a Multi-Core Compatible Linux Bootable 64-bit Out-of-Order RISC-V Processor Core | Sajin S, Shubham Sunil Garag, Anuj Phegade, Deepshikha Gusain, Kuruvilla Varghese (IISc, Bangalore)	Design and Analysis of Multibit Multiply and Accumulate (MAC) unit: An Analog In-Memory Computing Approach | Swetha A (Sri Sivasubramaniya Nadar College of Engg Chennai); Abhishek Upadhyay (X-FAB); Bhupendra Singh Reniwal (IIT Jodhpur)	Analog AI Hardware and Compute Ecosystem for Machine Learning at the Edge | Pratik Kumar | IISc	

1520 hrs	1540 hrs	Voltage Boosted Schmitt Trigger Sense Amplifier (VBSTSA) With Improved Offset And Reaction Time For High Speed SRAMs | Gaurav Saraswat, Anuj Parashar (Synopsys)	A 2.5 GHz, 1-Kb SRAM with Auxiliary Circuit Assisted Sense Amplifier in 65-nm CMOS Process | Rupesh D. Kadhao, Siddharth R. K., Nithin Kumar Y. B., Vasantha M. H. (NIT Goa); Devesh Dwivedi (Global Foundries)	Design of Embedded Vision System based on Zynq SOC | Singam Venkata Krishna Pratap Reddy, Namburu Banbhushan, Paladugu Venkatesh and Karukula Tirumala Krishna | JNTUK	
1540 hrs	**1600 hrs**	**TEA BREAK**			
Tracks Open		**Track 6A- Technical Track Advances in CAD & VLSI**	**Track 6B- Technical Track Analog & Mixed Signals-4**	**Track 6C- Student Research Forum**	**Track 6D-Start-up Forum**
1600 hrs	1620 hrs	Transport-Free Placement of Mixers for Realizing Bioprotocol on Programmable Microfluidic Devices | Masataka Hirai (Ritsumeikan University); Debraj Kundu (IIT Roorkee) ; Shigeru Yamashita (Ritsumeikan University); Sudip Roy (IIT Roorkee); Hiroyuki Tomiyama (Ritsumeikan University);	Invited Talk | Design and Analysis of In Memory Computing Architectures for Machine Learning Applications | Joycee Mekie, IIT Gandhinagar	Device modeling of oxide thin-film transistors | Ashima Sharma, Pydi Ganga Bahubalindruni and Manisha Bharti | NIT, Delhi	1600-1650 hrs : Startup Pitches | Sumedha IT | Anew Design Automation LightSpeed Photonics | VASBEAM | Cyrrup Solutions | Rapture Innovation Labs | Anscer Robotics | Hivericks Technologies | Vanix Technologies Spearix Technologies | Silizium Circuits | Krisemi Design Technologies 1650-1730 hrs : Roundtable Discussion
1620 hrs	1640 hrs	Efficient 3D Modeling Methodology for High-Speed Channels | Sivalingam Thirubalan (Microchip); Desmond Tan Hai Peng (Ansys); Suresh Kumar Kopparti (Microchip);	Common Mode Insensitive Process Tolerant Sense Amplifier Design for In Memory Compute Applications in 65nm LSTP Technology | Belal Iqbal, Anuj Grover (IIIT Delhi), Harsh Rawat (STMicroelectronics)	Fine-Grained Detection of Cache Side Channel Attacks | Pavitra Prakash Bhade |	
1640 hrs	1700 hrs	ISP: An Improved Slicing Pair Code for Skewed Slicing Floorplan | Biswojit Nayak, B. N. B. Ray (Utkal University)	Supply Noise and Peak Current Reduction in High-Speed Output Drivers | Dharmaray Nedalgi, Lavanya M. N (Intel); Saroja	Evolvable Hardware based approach to design Fault tolerant control circuit for FPGA based design | Deepanjali S and Dr. Noor	

			Siddamal (KLE Technological University)	Mahammad | IIIT, Kancheepuram	
1700 hrs	1720 hrs	Maximum Power Point Tracking using Buck-Boost converter for EH-PMIC | Sujata Kotabagi, Raghavendra Nayak, Sachin Dalabanjan, Vineet P N, Priyanka L. Patil, Sameer Hemadri (KLE Technological University)	An Energy-Efficient and Robust 10T SRAM based In Memory Computing Architecture | Noopur Srivastava, Anil Kumar Rajput, Manisha Pattanaik, Gaurav Kaushal (IIITM Gwalior)	Modelling of Antipode Attack in Bufferless NOC by Hardware Trojan | Josna VR, Rose George Kunthara, Neethu K and Rekha K. James | CUSAT	
1720 hrs	1740 hrs	GRILAPE: Graph Representation Inductive Learning-based Average Power Estimation for Frontend ASIC RTL Designs | Rakesh M B, Pabitra Das, Sai Pranav K R, Amit Acharyya (IIT Hyderabad)	Memristor-based High Speed and Area Efficient Comparators in IMPLY Logic | Nandit Kaushik, B. Srinivasu (IIT Mandi)		