Start (IST)	End (IST)	Duration	Track 1 (Intel | Octave-3 | Conf. Room, Flr-14, 1401/1402)	Track 2 (Silabs | Octave-3 | Conf. Room, Flr- 3, Training Room)	Track 3 (Intel |Octave-3| Conf. Room, Flr-14, BUM)
08:30	09:15	00:45	**Welcome/Registration to VLSID 2023**		
09:30	12:30	03:00	**1.1.1 Optimizations for Domain Specific MPSoC computing** Prof. Sri Parameswaran, University of New South Wales, Australia; Prof. Joerg Henkel, Karlsruhe Institute of Technology, Germany; Prof. Preeti Panda, IIT-Delhi, India; Assoc. Prof. Soumya J, BITS Pilani, Hyderabad, India	**1.2.1 Systematic design of Bandgap Voltage Reference Circuits** Prof Shouri Chatterjee, IIT Delhi Dr Rakesh Kumar Palani, Assistant Professor, IIT Delhi Prof Rajasekhar Nagulapalli, Oxford Brookes University, UK	**1.3.1 Neuromorphic Computing: Technologies, Architectures, Systems, and Compilers** Dr. Moritz Joseph, RWTH Aachen University, Germany Leticia Bolzani Poehls, RWTH Aachen University, Germany
12:30	13:30	01:00	**Lunch Break**		
13:30	16:30	03:00	**1.1.2 RISC-V : The Open Era of Computing** P R Sivakumar, Founder and CEO, Maven Silicon	**1.2.2 CMOS Clocking Technology for Wireline, Wireless and SoC Applications** Hormoz Djahanshahi, Associate Fellow, Microchip Technologies	**1.3.2 Hardware Design for Machine Learning [4 hrs]** Sandip Kundu, University of Massachusetts, Amherst, MA, USA

Start (IST)	End (IST)	Duration	Track 1 (Intel | Octave-3 | Conf. Room, Flr-14, 1401/1402)	Track 2 (AMD | Octave-2 | Conf. Room, Flr- 11, Design, Develop, Discover)	Track 3 (Intel |Octave-3| Conf. Room, Flr-14, BUM)
08:30	09:15	00:45	**Welcome/Registration to VLSID 2023**		
09:30	12:30	03:00	**2.1.1 CXL - high speed cache coherent interconnect** Sridhar Muthrasanallur, Principal Engineer, Intel, Bangalore, India Sunita Jain, AMD, Bangalore, India	**2.2.1 Building Energy Efficiency into Wireless IoT Semiconductor Devices** Venkatesh Narasimhan, Sr. Director of Engineering, Silicon Labs Joseph Kolapudi, Associate Engineering Mgr, Silicon Labs	**2.3.1 Functional Verification of Multichip Reference Design compute subsystem for Hyperscalar SoCs** Alok Sharma –Principal Engineer, ARM, Cambridge, UK. Vikash Chandra – Director Engineering, ARM, Bangalore, India Arulvasan Muniselvam – ARM, Bangalore, India
12:30	13:30	01:00	**Lunch Break**		
13:30	16:30	03:00	**2.1.2 Disaggregation Technology** Biswajit P: Senior Principal Engineer, Intel, Bangalore Deboleena S: Principal Engineer, Intel, Bangalore Rupesh P: Principal Engineer, Intel, Bangalore	**2.2.2 New era of Automotive Mobility** Dr Kostas Doris, Fellow, NXP Semiconductors & Professor at Technical University of Eindhoven, The Netherlands Preet Yadav, R&D SOC Technical Program Manager, NXP Semiconductors, India	**2.3.2 Quantum Computing: Algorithms, Systems and Design Automation** Assoc. Prof. Anupam Chattopadhyay (Nangyang Technical University, Singapore) Prof. Amlan Chakrabarti (Calcutta University, India) Prof. Susmita Sur-Kolay (Indian Statistical Institute, Kolkata) Prof. Robert Wille (Technical University of Munich, Germany) Assoc. Prof. Manas Mukherjee (Centre for Quantum Technology/NUS, Singapore)